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Three Dimensional Integration (3DI) of semiconductor circuit layers: new devices and fabrication process

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Three Dimensional Integration (3DI) of semiconductor circuit layers: New devices and fabrication process

by

Babak Sehari

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

Major: Electrical Engineering (Microelectronics)
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Ames, Iowa
1998

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INTRODUCTION

Three Dimensional Integration (3DI) is one of the most promising methods for increasing the number of devices per chip. In this technique, layers of circuits are built using Silicon On Isolator (SOI) technology. Then, these layers are stacked on top of each other and interconnected via Vertical Interconnects (VIs). There are three main original contributions in this paper for this technology:

- A new active device architecture for this technology is presented in Chapter 1 and further developed and verified in Chapters 5 and 6.

- A new inter-layer semiconductor shield to manage the problem of cross-talk between the layers is introduced in Chapter 2. Later this idea was further developed for analog and microwave circuits in Chapter 4. Effectiveness of this inter-layer shield is experimentally verified in Chapter 7.

- A new process for fabrication of this technology, based on newly developed technologies discussed in Appendix 1, is presented in Chapter 3. This process is verified using SUPREM computer simulation in Chapter 6.

To familiarize and refresh the reader with this work's foundations, a review of the special techniques for manufacturing semiconductor devices, related to 3DI technology, is presented in Appendix 1. To be inclusive, this Appendix compares this technology with rival technologies, i.e. Wafer Scale Integration (WSI) and Ultra Large Scale Integration (ULSI). One can conclude based on the materials presented in this Appendix that 3DI is more promising than the other two technologies.

Chapter 1 is devoted to the selection and design of the most appropriate device that can meet the stringent requirements of 3DI technology. The compatibility of currently used devices

with a 3DI technology is presented first. Then, a new device architecture is proposed for this technology. Finally, a theoretical analysis of the characteristics of this device is presented.

Chapter 2 is devoted to analyze and solve the important problems associated with this technology. This chapter includes discussions about inter-layer cross-talk and appropriate shield design to overcome this problem. Other significant issues related to 3DI technology presented in this chapter are: the heat dissipation of a 3DI chip and appropriate device isolation methods for this technology.

In Chapter 3 a review of variety of approaches to create a practical 3DI chip is presented. Then, a fabrication procedure for 3DI technology based on the technologies that was reviewed in Appendix 1 is proposed.

Chapter 4 deals with the issues concerning analog circuits fabricated based on 3DI technology. This chapter examines construction of passive elements, such as inductors, in several closely packed semiconductor layers environment. Further more, the issues concerning 3DI microwave circuits are investigated.

Choosing practical materials for the device presented in Chapter 1 is the subject of study in Chapter 5. Numerous metals and metal-silicides are investigated for selection of correct metal-semiconductor or [metal-silicide]-semiconductor ohmic contact for both n-type and p-type semiconductors. Also, the "aging" of such contacts are investigated.

Chapter 6 is intended to utilize computer simulation to verify the 3DI processing steps presented in Chapter 3. SUPREM simulation is utilized to examine several cross section of the processing steps. Furthermore, widely accepted Finite Difference Method (FDM) is utilized to verify the active device designed for 3DI technology in Chapter 1 and Chapter 5.

Experiments designed for verification of the inter-layer shield along with discussion of the results is presented in Chapter 7. As it will be fully discussed in this chapter, two sets of double sided polished wafers of the same thickness were used to verify our theoretical results obtained in chapter 2. In one set of wafers we diffused Phosphorous in one side of the silicon

wafers to create a highly doped layer with thickness of a few μm. The other set of wafers were left undoped. The measurement showed that this shallow layer of highly doped silicon reduced the cross talk problem to an acceptable level.

The overall conclusions are presented in the final chapter of this paper.

1. DEVICE ARCHITECTURE FOR 3DI TECHNOLOGY

A review of 3DI requirements and the latest developments in its related technologies is presented in the Appendix. Moreover, it has been mentioned in the Appendix , that one of the biggest problems associated with 3DI technology is the possibility of redistribution of impurities in lower layers when the substrate is heated to build the upper layers. As a result, strenuous temperature requirement and other processing conditions are placed on each processing step. These conditions can be eased by designing new devices that are more compatible with 3DI technology. These devices should be more resistant to the environments that are required for production of the upper layers. Therefore, these new devices should impose less restrictive conditions on the processing steps.

In this chapter the focus is on the devices. First, the compatibility of conventional devices with 3DI technology is evaluated. Then, new devices for 3DI technology will be presented and explained.

1.1 Conventional Devices and 3DI Technology

Conventional devices, such as MOSFETs and bipolar transistors, are not particularly designed for use in 3DI technology. In order to employ these devices in a 3DI technology, extremely strenuous conditions should be imposed on each process of manufacturing. To better comprehend this, let us consider two of the most popular active devices used in today's technology.

1.1.1. Bipolar Transistors and 3DI Technology

The bipolar transistor is the first device to be considered here. This device was more popular in the past and is still being used extensively in different IC technologies (such as TTL, ECL, and many analog technologies).

In most bipolar transistors, the base region is only less than 1 μm thick. Nevertheless, this region is the most important part of a bipolar transistor; a small change to the thickness of this region and in its impurity concentration relative to the other two regions can change the characteristics of the device considerably. This can also be observed from the formula used for calculating the gain of a bipolar transistor: [1]

$$\beta_o \approx h_{FE} \approx \frac{N_E}{N_B W} \approx \frac{N_E}{Q_b} \quad \text{Eq. 1.1}$$

N_E = Emitter Doping.

N_B = Base Doping.

W = Undepleted Width of the Base region.

$$Q_b = \int_0^W N(x)dx \quad (Q_b \text{ is called Gummel number}) \quad \text{Eq. 1.2}$$

N(x) is the base impurity distribution

As can be seen in this equation, a small change to the base impurity level leads to large variation in the gain of the transistor. With this in mind, let us examine the doping profile of a typical bipolar transistor that is shown in Fig. 1.1. It can be observed from this figure that a heavily doped emitter region is next to a relatively lightly doped base region. This is done to increase the transistor gain as explained in the above equations. Therefore, any heating steps required for manufacturing of the upper layers can cause the impurities from emitter region to migrate to base region, resulting in a change in the impurity concentration of the base and its effective width. Moreover, the impurity of the base region, which is at a higher level than the collector region, can diffuse into the collector region making the transistor gain more suseptable to collector voltage. Here, note that the collector's n^+ region shown in Fig. 1.1 (which is used to reduce series resistor) can defuse and cause problem in a bipolar transistor.

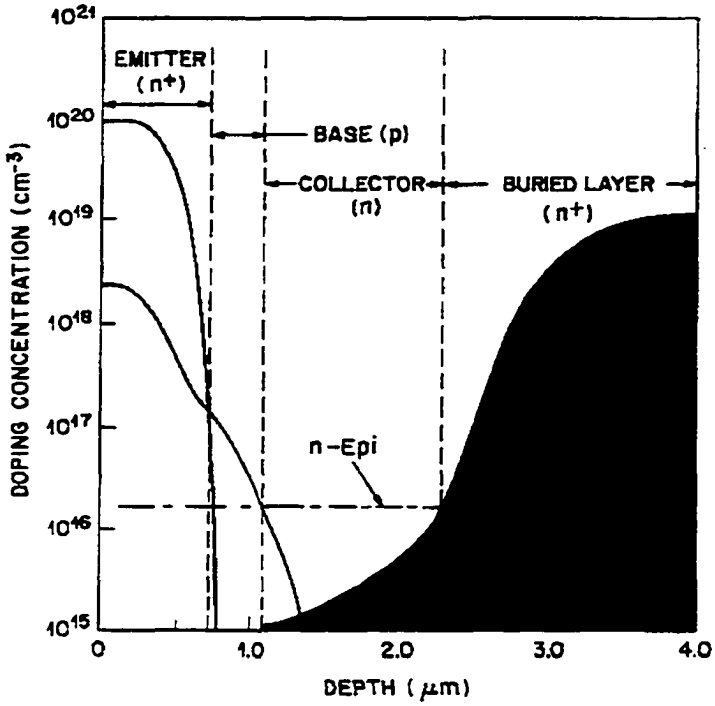


Fig. 1.1. Doping profile of a typical bipolar transistor.[2]

The simple analysis presented above shows that bipolar transistor is not suitable for 3DI technology; therefore, other active amplifying devices should be examined for this technology.

1.1.2. MOSFET and 3DI technology

The other popular device currently used in semiconductor industry is MOSFET. Analogous to bipolar transistor, MOSFET, is highly vulnerable to the redistribution of impurities which can occur as a result of high temperatures needed to build upper layers. This fact can be observed from Fig. 1.2. As it can be seen in this figure, a relatively lightly doped gate is located in-between two heavily doped regions of the device (source and drain). Moreover, the gate's doping is of the opposite kind of impurity than the other two regions. Therefore, the high temperature used to build upper layers can cause the impurities inside the

source and drain to diffuse into the gate and then dope it with opposite impurity. This means the source and drain boundaries move closer to each other. The closer proximity of the source and drain can cause the depletion regions of the source and the drain to touch each other, causing device to malfunction. Furthermore, the characteristics of FETs are heavily influenced by the gate length. With reduction in the gate length, the device parameter changes sharply. Of course, MOSFETs with smaller gate lengths are more vulnerable to the redistribution of impurities than MOSFETs with larger gate lengths, as can be concluded from Fig. 1.2.

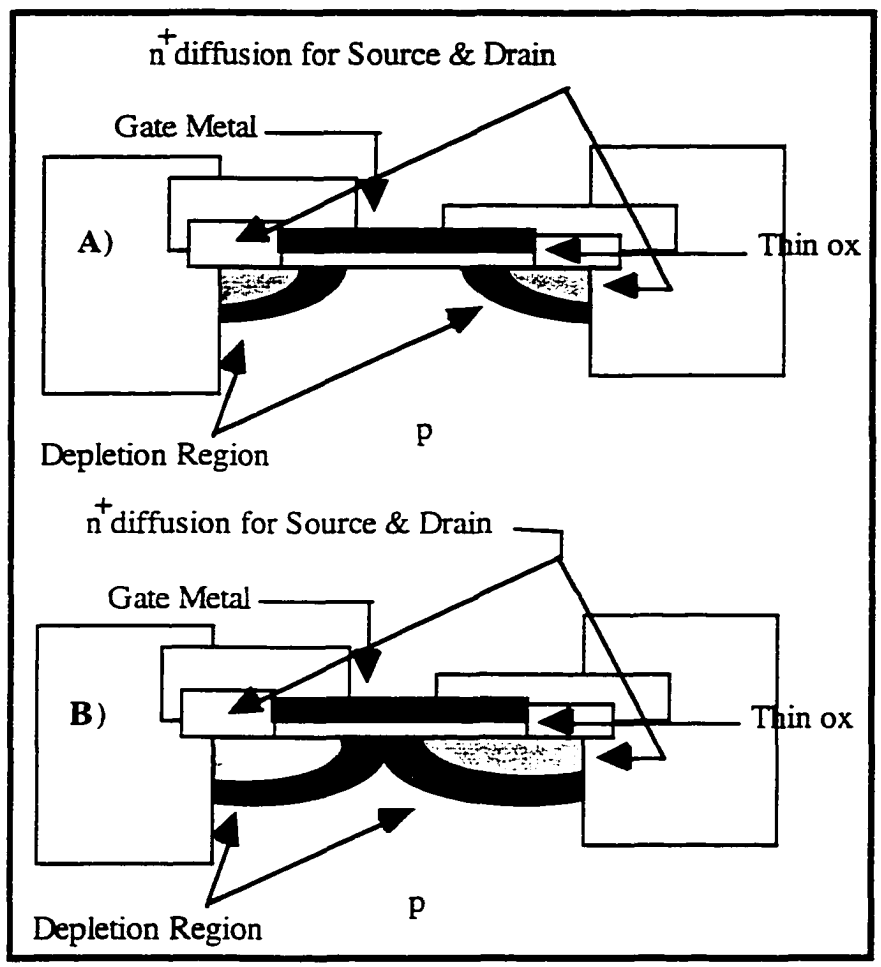


Fig. 1.2. N-channel MOSFET. A) normal MOSFET. B) the source and drain impurities have diffused into gate region. As a result, the B device is not functioning correctly.

1.2. New Devices and 3DI technology

In the quest to design a device that is more compatible with possible 3DI technology, many types of transistor architectures were considered. At first glance, the devices designed for sub-micron technology, such as UMOS[3] and VMOS[4], looked very promising. However, these devices require many processing steps and make the surface of the substrate jagged. Therefore, an extensive planarization step should be undertaken after production of each layer. It is common knowledge that as the number of steps increases, the over all yield decreases. As a result, it is very important to reduce the number of processing steps as much as possible, especially for 3DI technology. One comes to this conclusion because each processing step for building each layer should be repeated n times for a n layer structure. In addition, these architectures require many types of impurities with different concentrations to be present on each device. These impurities are still vulnerable to redistribution as a result of high temperatures used for building the upper layers.

On the other front, Metal-Semiconductor Field Effect Transistor (MESFET) is the device of choice in GaAs technology. This is due to GaAs' high resistance that acts as an insulator. Moreover, GaAs Oxide has undesirable characteristics. A closer look at MESFET reveals that this device uses only one type of impurity; therefore, the redistribution of impurities within the device does not disturb the device. In addition, there is no sensitive thinox region in the MESFET, which would eliminate the concerns of high temperature effects for such region. Finally, it only takes very few processing steps to build this device, which should lead to higher production yield. These characteristics inspired me to use the structure of this device as a reference for designing a 3DI compatible device.

1.2.1. SOI Schottky Barrier Field Effect Transistor (SOI-SB-FET)

The predicaments associated with manufacturing of the popular semiconductor devices, such as BJT, and MOSFET provided the incentive to design a more suitable device for 3DI

technology. Since the 3DI technology uses layers of Silicon On Insulator as the building blocks, the device is designed to take advantage of this feature of 3DI technology. Secondly, in order to reduce the likelihood of damage to the device, the device should have as few regions of impurity as possible. That is, a device with two different impurity regions is better than one with three different impurity regions. Therefore, a device with one impurity region is the most favorable device for 3DI technology. To accommodate these constraints, the following device is suggested by this paper.

Fig. 1.3 presents a schematic view of this device. As it can be seen from this figure, a piece of metal is placed on top of an SOI layer creates the device similar to MESFET on GaAs. The device that could be isolated by various means, such as oxidized ring guard or ring Schottky barrier. These methods will be discussed later. Of course, the metal could be replaced by metal-silicides and other changes should be made (such as placement of metal diffusion barrier under the metal) to made this device truly compatible with 3DI technology.

The depletion region created by Schottky barrier limits the height of the channel and as a result controls the follow of electrons from source to drain. By application of various potentials to the gate metal with respect to the channel the height of the depletion region can be controlled. In following sections, the relation between this potential and the height of the depletion region, along with the other characteristics of this device, will be investigated.

1.2.2. The Physics of SOI-SB-FET

At this point , let's take a closer look at this device. The Schottky barrier is the most important concept in this device. The true understanding of this device is not possible without a good understanding of the Schottky barrier; therefore, a review of the Schottky barrier phenomenon is presented in the next section.

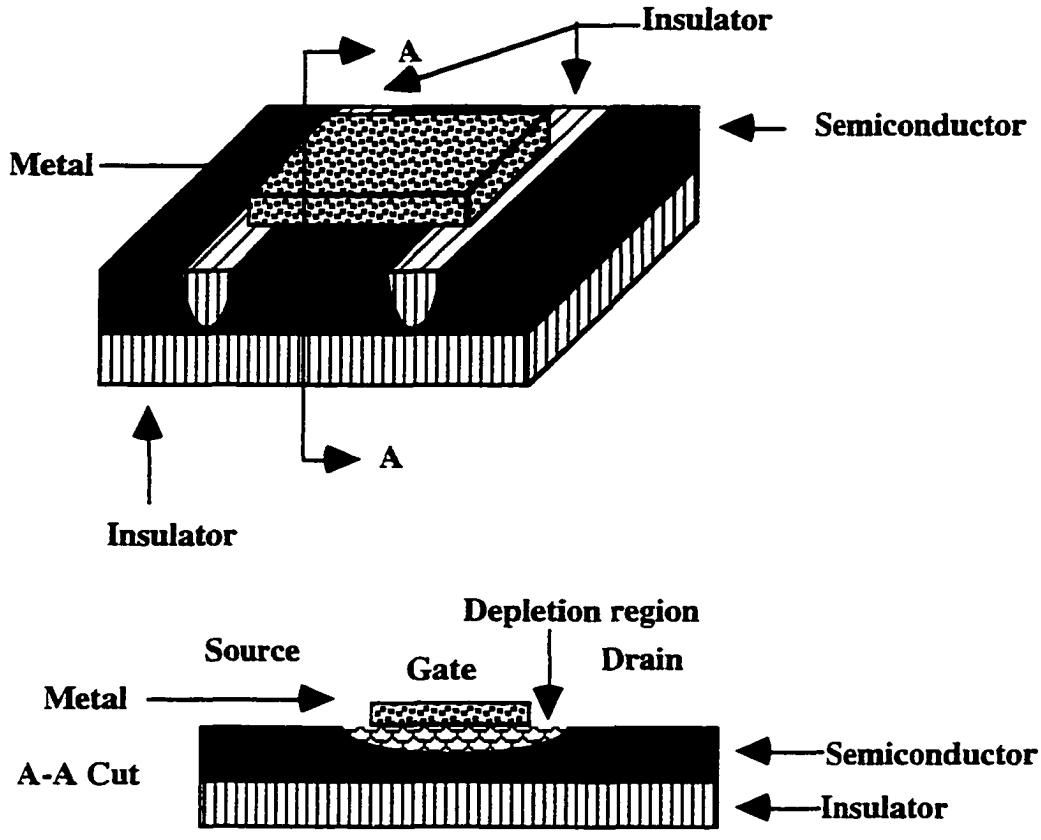


Fig. 1.3. Schematic diagram of a SOI-SB-FET

1.2.2.1. Schottky Barrier in SOI-SB-FET

To investigate this subject, first let's review a few of the key terms. The first important term in this area is the metal's work function (Φ_m). The metal's work function is defined as the energy required to lift an average electron (an electron in Fermi level) from the surface of the metal to the vacuum surrounding it. This energy can be calculated using quantum mechanics.[5] There are two main contribution to this energy: volume contribution and surface contribution.[6] The volume contribution is related to electron's energy due to the periodic potential of metals. This energy has to do with how the metal's electron orbitals are filled at natural state. The surface contribution is related to the existence and the state of dipoles at the surface of the metal.[7]

It is obvious that if the surface condition of a metal changes, the contribution of this factor changes, as well. Such alterations may also come about as a result of the adsorption of a gas or other materials by the metal's surface. Moreover, the crystallographic orientation of a metal can change the dipole forces on the surface of the metal. This results in a change to the surface contribution of the metal's work function. Tungsten, for instance, is known to have the work function of equal to 4.47 eV in (111) surface, 4.63 eV in (100) surface, and 5.25 eV in (110) surface.[6] However, for practical purposes this energy is measured by methods such as photoelectric phenomenon.[5]

An analogous term *work function* is defined for the semiconductors, too. The *semiconductor's work function* (Φ_S) is defined as the energy difference between an imaginary electron at Fermi level and an electron at the vacuum (infinity) level. One should note that except for degenerate semiconductors, the Fermi level of a semiconductor is in the forbidden band gap. Therefore, in reality no electron can be found at the Fermi level of a semiconductor. However in statistical or macro point of view , the weighted average of the electrons' energies in a semiconductor is equal to the Fermi level of that semiconductor. Consequently, "the weighted average of the energies necessary to remove an electron form the valence and conduction bands"[6] is defined as the work function of a semiconductor.

Electron affinity (χ_S) is another important semiconductor parameter that will be seen in this study, time and time again. This term is defined as *the energy required by an electron at the bottom of conduction band for it to break free* from the semiconductor. This entity, like the work function, is susceptible to the surface condition of the semiconductor.[6]

Finally, let's define ξ to be the potential difference between Fermi level and the bottom of the conduction band. That is:

$$\xi = \Phi_C - \Phi_F = \frac{E_C - E_F}{q} \qquad \text{Eq. 1.3}$$

Where E_C is the energy level at the conduction band, E_F is the Fermi energy level, Φ_C is the potential of the conduction band, Φ_F is the potential at the Fermi level, and q is the charge of an electron. The value of ξ could be calculated based upon the impurity concentration of semiconductors. For n-type semiconductor, this value equals to:[8]

$$\xi = \frac{E_C - E_F}{q} \approx \frac{KT}{q} \text{Ln}\left(\frac{N_C}{N_D}\right) \quad \text{(For n-type)} \qquad \boxed{\text{Eq. 1.4}}$$

Similarly, for p-type this value could be calculated as:[8]

$$\xi = \frac{E_C - E_F}{q} = \frac{(E_C - E_V) - (E_F - E_V)}{q} \approx \frac{E_g}{q} - \frac{KT}{q} \text{Ln}\left(\frac{N_V}{N_A}\right) \quad \text{(For p-type)}$$

$$\boxed{\text{Eq. 1.5}}$$

Where E_V is the valence band energy level, E_g is the energy gap of the semiconductor, K is the Boltzmann's constant, T is the absolute temperature in ^oK, N_V is the effective density of states in the valence band, N_C is the effective density of states in the conduction band, N_A is the concentration of acceptor impurities, and N_D is the concentration of the donor impurities in the semiconductor. Fig 1.4 is a schematic representation of various energies defined so far.

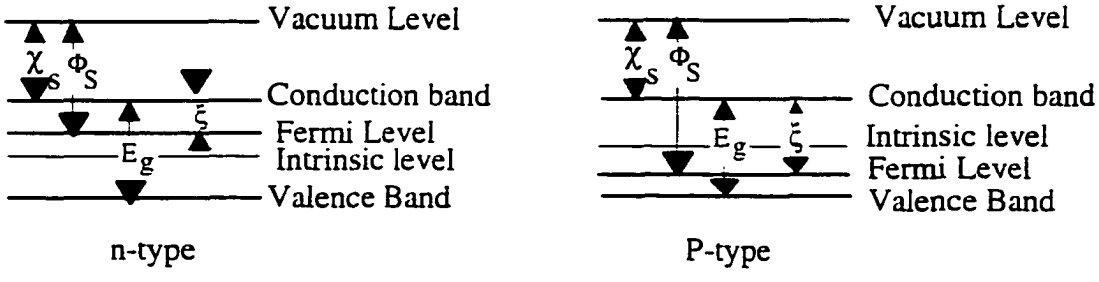


Fig. 1.4. Schematic diagram of the different energy concepts in a semiconductor.

Therefore, as it can be seen from Fig. 1.4. the work function of a semiconductor can be calculated as follows:

$$\Phi_S = \chi_S + \xi \quad \boxed{\text{Eq. 1.6}}$$

Now let's see how the energy-band diagram adjust itself when a semiconductor and a metal make a contact. The explanation that follows is based on the Schottky theory of metal-semiconductor contact. According to this theory, the Fermi Level of semiconductor aligns itself with the Fermi level of the metal. This result occurs because to the fact that both materials exchange electron until they reach thermal equilibrium. The metal electrons can move freely inside metal; therefore, any loss or gain of electrons at the contact site is shared with the rest of the metal. However, when the area adjacent to the contact in the semiconductor losses or gain electrons; it creates immobile charges at that area. These immobile charges, which are located close to the contact surface, form an electric field that prevents the further transfer of electrons between the two materials. As mentioned before, the Fermi levels have to be aligned. To compensate for this alignment, the other energy levels bend as result of the electric field. An example of a space-energy diagram for both the n-type and the p-type semiconductor is given in Fig. 1.5.

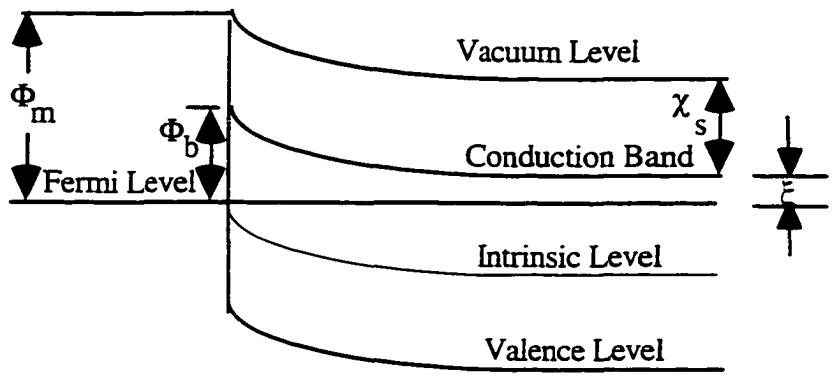
As can be concluded from the Figure 1.5, the height of the barrier between a n-type semiconductor and a metal can be calculated as follows:

$$\Phi_b = \Phi_m - \chi_S \quad \boxed{\text{Eq. 1.7}}$$

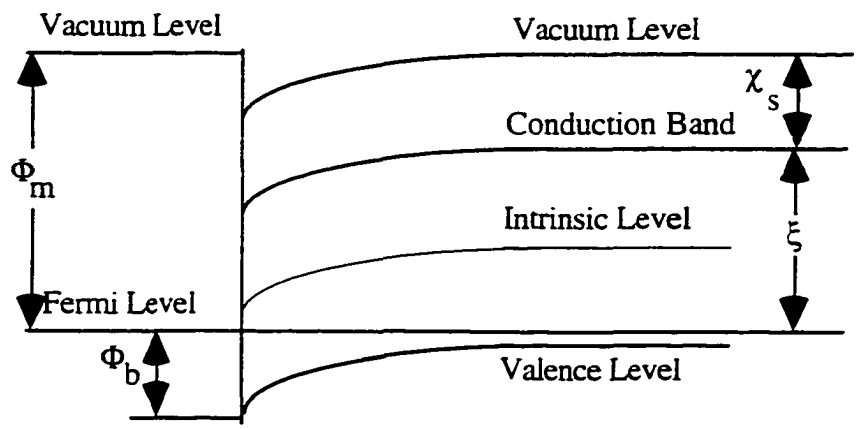
This equation is due to the fact that in the n-type semiconductor electrons are the majority carriers, which are mainly responsible for the current transport. Moreover, the weighted average of the electron energies inside the semiconductor is equal to the Fermi level. Therefore, an electron should have energy $q\Phi_b$ higher than an electron with an average energy

to be able to travel from the semiconductor side to the metal side.

Of course, this is a rough estimate of the value of this barrier. There are other factors involved for determing for a more accurate calculation of barrier heights. Two such important considerations are the Schottky effect[9] (which tends to lower barrier heights as a result of image charges[10]) and the effect of interface charges.



n-type semiconductor metal contact



p-type semiconductor metal contact

Fig. 1.5. Space-energy diagram for a n-type (top) and a p-type (bottom) semiconductor-metal contact.

The Schottky effect in lowering the barrier height could be calculated as:[9]

$$\Delta\Phi = \sqrt{\frac{qE}{4\Pi\varepsilon_S}} \quad \text{Eq. 1.8}$$

where E is the external electric field (here it is assumed that external electric field is much larger than the electric field generated by Schottky contact) and ε_S is the semiconductor's static permittivity. Fig 1.6 presents a graphical view of the barrier lowering as a function of square root of external electric field for Au-Si contact.[9]

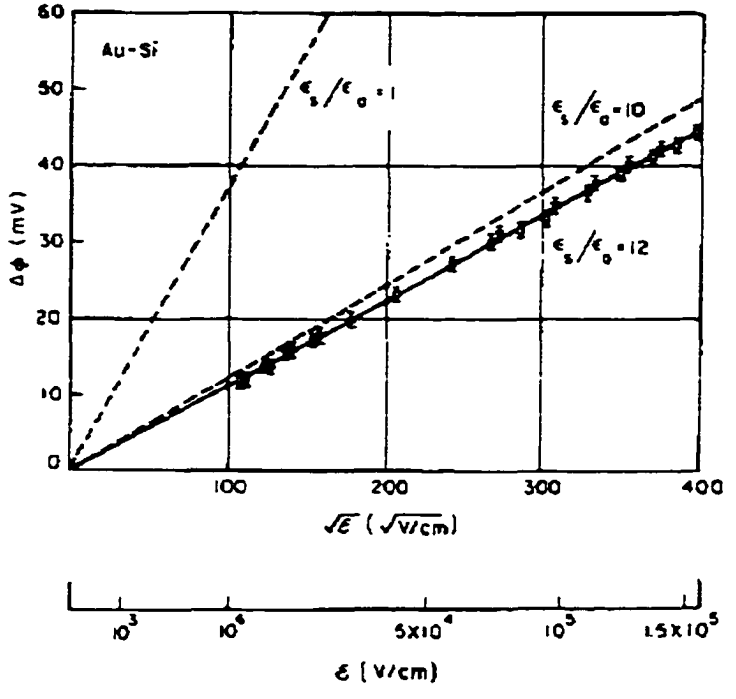


Fig. 1.6. Measurement of barrier lowering as a function of the electric field in a Au-Si diode[9]

Evidence in Figure 1.6 combined with the fact that most barriers useful to this study are one to two order magnitude larger than barrier lowering under practical situations, show that the effect of barrier lowering is insignificant for proposes of this study.

Similar argument could be made for p-type semiconductor; Although, one should keep in mind that the carriers in this type of semiconductor are the holes. As a result, the barrier height for a p-type semiconductor can be calculated as follows:

$$q\Phi_b = E_g - q(\Phi_m - \chi_S) \quad \text{(For p-type semiconductor-metal contact)} \qquad \text{Eq. 1.9}$$

This equation can be explained using Fig. 1.5. As can gathered from this figure, an average hole's energy should increase $q\Phi_b$ to be able to overcome the energy barrier. Also, note that the energy of a hole increases downward in Fig 1.5.

By comparing the equations given for calculation of p-type and n-type semiconductor-metal contact, it can be concluded that the sum of the barrier heights for a particular metal with n-type and p-type of one semiconductor should be equal to the the band gap of that semiconductor. That is:

$$E_g = q(\Phi_{bn} + \Phi_{bp}) \qquad \text{Eq. 1.10}$$

1.2.2.2. Ohmic vs. Rectifying Metal-Semiconductor Contacts

When a semiconductor and a metal make a contact there are two different types of contacts may result. One type has rectifying characteristics and the other is very similar to an ohmic contact.

Metal-semiconductor ohmic contact has characteristics very similar to an ohmic resistor. A good metal-semiconductor ohmic contact has low resistance that is constant under forward or reverse polarity. Both n-type and p-type semiconductors are capable of producing ohmic contacts. To have an ohmic contact in a n-type semiconductor, the metal's work function

should be less than the semiconductor's work function. However, in order to have an ohmic contact in a p-type semiconductor, the work function of the semiconductor should be less than the work function of the metal.

Similarly, both n-type semiconductors and p-type semiconductors can make rectifying contacts with metals. In this case, the n-type semiconductor should have a lower work function than metal while the p-type semiconductor should have higher work function than the metal to make a rectifying contact with metals. A synopsis of all these cases are shown in Fig 1.7.

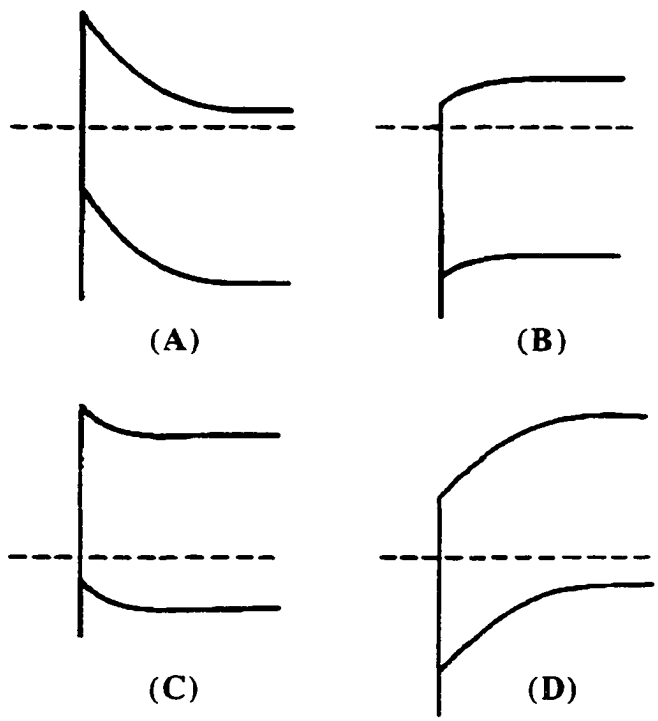


Fig. 1.7. Barriers for semiconductors of different types and work functions. n-type: (A) $\Phi_m > \Phi_S$ (rectifying); (B) $\Phi_m < \Phi_S$ (ohmic). p-type: (C) $\Phi_m > \Phi_S$ (ohmic); (D) $\Phi_m > \Phi_S$ (rectifying).[10]

Of course, the behavior of the ohmic contact can be explained as follows with the help of Fig 1.7. In Fig 1.7. (B) if the contact is biased in such a manner that electrons flow from semiconductor to metal, there is no barrier in its path. On the other hand, if the contact is biased so that electrons follow from the metal side to the semiconductor, the high concentration of electrons near the contact (which had caused the bands to bent downwards and is called the accumulation region) acts as a cathode providing ample amount of electron. In this case the resistance is determined by the bulk resistance of the semiconductor.[10] A similar argument can be made for holes of the Fig 1.7 (C), which is a p-type ohmic contact.

In this study, both the rectifying contact and the ohmic contacts are of interest. The rectifying contact is utilized for gate contact; whereas the ohmic contact is utilized as source and drain contacts to outside world.

1.2.2.3. Depletion Layer in a Metal-Semiconductor Contact

So far, the condition for creation of Schottky barrier has been reviewed. Now, it is time to calculate the depth of the depletion region in a metal-semiconductor contact. It should be noted that not all metal-semiconductor contacts create a depletion region, as explained in previous section.

The Schottky theory assumes that in metal-semiconductor contact, the majority carriers of the semiconductor adjacent to the contact site may migrate to the metal. This migration leaves the atoms of semiconductor adjacent to the contact site charged. For example, when the electrons migrate from the n-type semiconductor to a metal, the donor atoms near the contact lose their electron in this process. Therefore, they are positively charged. These charged atoms create an electric field that prevents further movement of electrons from semiconductor to metal. However, such a charged region in the metal side will be on the surface of the metal in order to cancel any electric field inside the metal. This design is based on the electric field inside the metal which is always zero. Fig 1.8 presents a graphical view of the charged region

for both the n-type and p-type of semiconductors. The stationary charges are shown inside a circle. Looking at Fig 1.8, one oberves that the stationary charges in an n-type semiconductor are positive donor atoms and the stationary charges in p-type semiconductor are negative acceptor atoms.

To get a mathematical view of this phenomenon, let's apply the Poisson's equation to the metal-semiconductor contact. General Poisson's equation could be written as:

$$-\frac{\delta^2 \Phi_x}{\delta x^2} = \frac{\rho_{(x)}}{\varepsilon_S} \qquad \text{Eq. 1.11}$$

Applying this equation to the charged region where N_B is equal to the concentration of donors(N_D), in a n-type semiconductor, or acceptors(N_A), in the p-type semiconductor:

$$\frac{\delta\left(-\frac{\delta \Phi}{\delta x}\right)}{\delta x^2} = \frac{qN_B}{\varepsilon_S} \quad (0 < x < h) \qquad \text{Eq. 1.12}$$

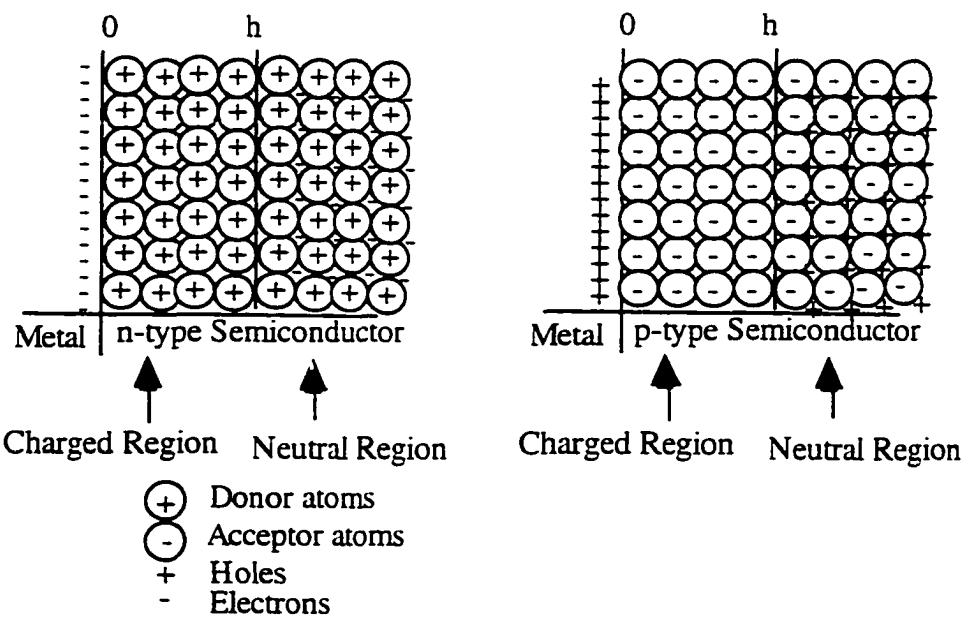


Figure. 1.8. Charged distribution of n-type and p-type semiconductor-metal depletion contact.

$$\int \delta \left(- \frac{\delta \Phi}{\delta x} \right) = \int \frac{qN_B}{\varepsilon_S} \delta x \quad \boxed{\text{Eq. 1.13}}$$

Assuming the doping density is uniform in this region:

$$- \frac{\delta \Phi}{\delta x} = \frac{qN_B x}{\varepsilon_S} + C \quad \boxed{\text{Eq. 1.14}}$$

applying the limits of integrations to the above equation:

$$\left[- \frac{\delta \Phi}{\delta x} = \frac{qN_B x}{\varepsilon_S} + C \right]_0^h \quad \boxed{\text{Eq. 1.15}}$$

$$- \left[\left[- \frac{\delta \Phi}{\delta x} \Big|_h \right] - \left[- \frac{\delta \Phi}{\delta x} \Big|_0 \right] \right] = \frac{qN_B h}{\varepsilon_S} \quad \boxed{\text{Eq. 1.16}}$$

$$- [E_{(h)} - E_{(0)}] = \frac{qN_B h}{\varepsilon_S} \quad \boxed{\text{Eq. 1.17}}$$

At x=h, where the semiconductor charges are not disturb any more under Schottky model, $E_{(h)} = 0$. Therefore:

$$| E_{max} | = | E_{(0)} | = \frac{qN_B h}{\varepsilon_S} \quad \boxed{\text{Eq. 1.18}}$$

Let's continue to calculate the potential of the barrier height[1]:

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[1] Logically, the image forces $\left(E(x) = \int_{\infty}^{x} F \partial x = \frac{q^2}{16 \pi \varepsilon_0 E} \right)$ can be added to the total electric field; however, doing so complicates the problem by creating a third order equation in terms of x. Moreover, as it has been shown before, the image forces have a minimal effect on the over all barrier height. Therefore as a first aproximation, it will be ignored.

$$-\frac{\delta\Phi}{\delta x} = \frac{qN_B x}{\varepsilon_S} \quad \text{Eq. 1.19}$$

$$\int -\delta\Phi = \int \frac{qN_B x}{\varepsilon_S}\delta x \quad \text{Eq. 1.20}$$

$$\Phi = -\frac{qN_B}{2\varepsilon_S} x^2 + C \quad \text{Eq. 1.21}$$

$$-[\Phi]_0^h = \left[\frac{qN_B}{2\varepsilon_S} x^2 + C\right]_0^h \quad \text{Eq. 1.22}$$

$$-[\Phi_h - \Phi_0] = \frac{qN_B}{2\varepsilon_S} h^2 \quad \text{Eq. 1.23}$$

The left side of the last equation describes the potential difference between point x = h and point x= 0. This potential difference is the sum of all the contributions from the different source. Therefore, this includes the external potential applied to this junction[2] V_f, the majority-carrier contribution,[3] which is equal to $\frac{KT}{q}$, and the barrier height at natural state Φ_b.

$$-[-\Phi_b + V_f + \frac{KT}{q}] = \frac{qN_B}{2\varepsilon_S} h^2 \quad \text{Eq. 1.24}$$

Therefore, the depth of this region could be calculated as:

$$h = \sqrt{\frac{2\varepsilon_S}{qN_B}[\Phi_b - V_f - \frac{KT}{q}]} \quad \text{Eq. 1.25}$$

This argument is equally valid for both the n-type and the p-type semiconductor contacts with metals.

---

2 The external potential is considered to be positive in forward direction and negative in backward directions.

3 This comes about as a result of taking the majority carriers along with the impurity contributions[9], that is $\rho = -q[N_A - p(x)]$.

1.3. Complementary MES (CMES) Circuits

One careful look at the equation given for the h in previous section suggest that PMES and NMES can be used in a setup similar to PMOS and NMOS in a CMOS circuit to form a Complementary MES (CMES) technology. However, the characteristics of MESFETs are different from those of MOSFETs'. This warrants a closer examination of CMES technology.

One method of connecting MES devices to form Complementary MES has been patented by E. T. Lewis.[11-12] The circuit for simple invertor using CMES technology is presented in Fig. 1.9.

Certainly, one of the biggest problems associated with this design is the forward voltage applied to the gate which should be less than the metal-semiconductor barrier height. Since, the input voltage of one stage in a digital IC is the output stage of previous stage, and the fact that the output voltage swings between the supply voltage and the ground; therefore, the supply voltage should be less than barrier height in order to prevent short circuiting the forward bias of the gate source junction. Most practical metal-semiconductor junctions have a barrier height of around 0.5 Volts. This means the supply voltage should be around 0.5 Volts, too. However, low supply voltage levels leads to low signal to noise ratio, due to noise generated by other sources. Therefore, this circuit should be well shielded to reduce the noise level as much as possible.

A few simple modifications to this circuit can make it possible for this technology to have a higher supply voltage. These modifications can generate several circuits, such as those shown in Figure 1.10. It can be seen from the circuits shown in this figure that in circuit A two diodes (which can be Schottky diodes) are utilized in series with the input of transistors to increase the maximum input voltage. In Circuit B, two other MESFETs are utilized as Schottky diodes to increase the input voltage. Finally, in circuit C four resistors are utilized as two voltage dividers to reduce the input voltage.

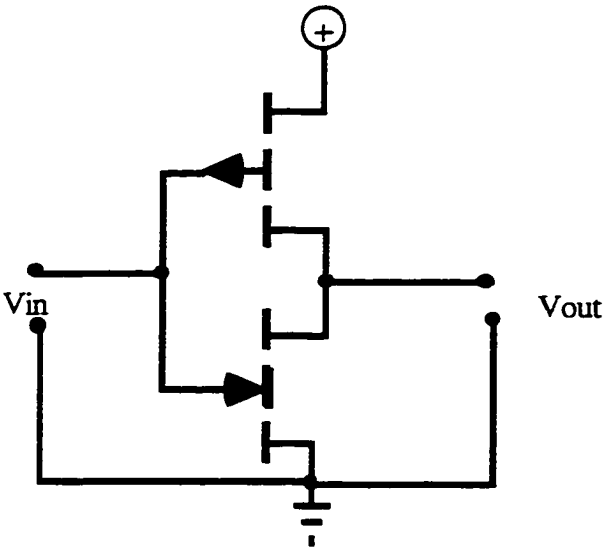

Figure. 1.9. CMES Invertor circuit, using two enhancement mode MESFET.[11-12]

Each of these techniques, designed to increase the input voltage tolerance of the MES circuits, has some advantages and some disadvantage. Here, let's compare their merits:

The circuits shown in Figure 1.10 A and B are simple circuits. These configurations can increase the input voltage tolerance of the circuit by built-in diode voltage. These diodes can be either PN junction diodes or Schottky diodes. The main problems associated with this type of circuit is the fact that the diodes take valuable space on the wafer. Moreover, in this technique the input voltage tolerance can be raised in steps only by a fixed amount, which is equal to the built in voltage of the diode. Of course, more series diodes can be utilized to further increase the input voltage tolerance; however, in that case most of the space on the wafer will be used by these diodes.

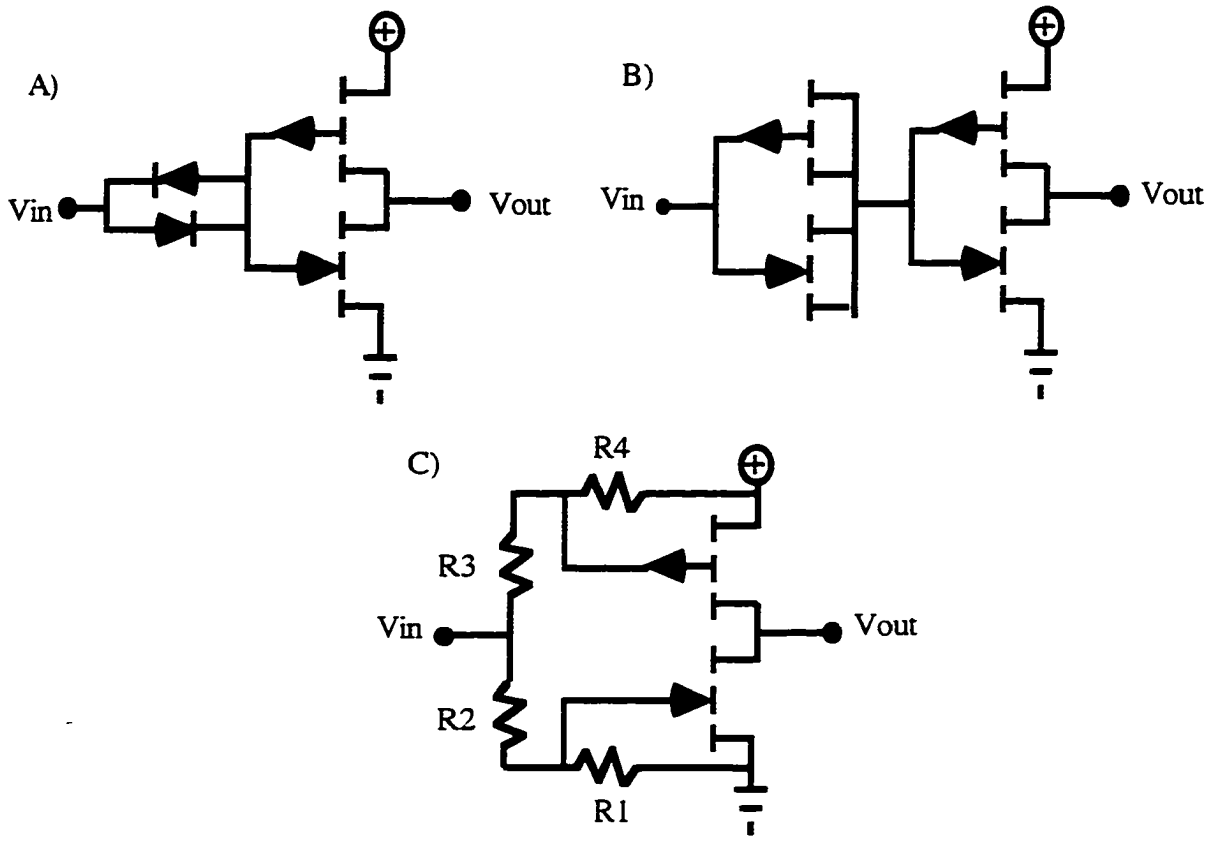

Figure. 1.10. Various circuits to increase the input voltage tolerance of a CMES circuits. (A) Using diodes the input voltage tolerance can be raised by the built in voltage of the diodes. (B) The Schottky diode of the gate source (drain) could be used similarly. (C) The resistor's voltage divider configuration can be utilized to increase the input voltage tolerance of the circuit.

The technique shown in Fig. 1.10. (C) can raise the input voltage tolerance of the circuit by any amount. The maximum V_{GS} for the upper transistor can be calculated as:

$$V_{GS} = \frac{R_4}{R_3 + R_4} V_{CC} \quad \boxed{\text{Eq. 1.26}}$$

Similarly, the maximum V_{GS} for the lower transistor can be calculated as:

$$V_{GS} = \frac{R_1}{R_1 + R_2} V_{CC} \quad \boxed{\text{Eq. 1.27}}$$

Note that in these calculations an assumption is made that the input of the previous logic layer is also a similar MESFET configuration; therefore the input voltage could vary between 0 to V_{CC}.

The disadvantages of this technique can be itemized as follows:

1. The resistors on this circuit take up large space.
2. The resistors consume energy and dissipate it, increasing the total energy dissipation of the chip.
3. The large resistors can act as several antennas and increase the noise level in the circuit.

Moreover, one should be reminded that the lower the supply voltage in an IC, the lower the energy dissipation of that IC. For example, a chip with a 5V power supply dissipate 100 times more power than a chip with 0.5V power supply, working under the same conditions. This is explained by the fact that the power is a quadratic function of voltage. ($p = \frac{V^2}{R}$)

An other consideration in a low voltage environment is noise. Of course, the designers of this type of circuit should take all usual precautions to minimize the effects of noise on the signal. For example, the IC package could be made of highly conductive metallic material. Note that layer to layer noise (i.e. "cross-talk", which will be considered thoroughly in the next chapter) is proportional to the line voltages; therefore, the lower the line voltage the lower the cross talk. Also note that in digital circuits noise tolerance is higher than analog circuits.

1.3.1. MESFET's Work Equations

It has been established that the MESFETs are better suited for 3DI technology. Therefore, a good mathematical understanding of the physics of this device is essential for any serious design work with this device. To analyze any semiconductor device at low

frequencies, one should start with Poisson's equation. However, this step has already been carried out in section 1.2.2.3. The result of this analysis has shown that the depth of metal-semiconductor depletion region can be calculated as:

$$h = \sqrt{\frac{2\varepsilon_S}{qN_B}\left[\Phi_b - V_f - \frac{KT}{q}\right]} \qquad \text{Eq. 1.28}$$

Here, V_f is the external bias of the metal-semiconductor junction (V_f is positive for forward direction and negative for backward direction), Φ_b is the barrier height of metal-semiconductor junction, and N_B is the concentration of impurities in the semiconductor (assumed to be constant). Now, let's consider the MESFET, shown in Fig 1.11.

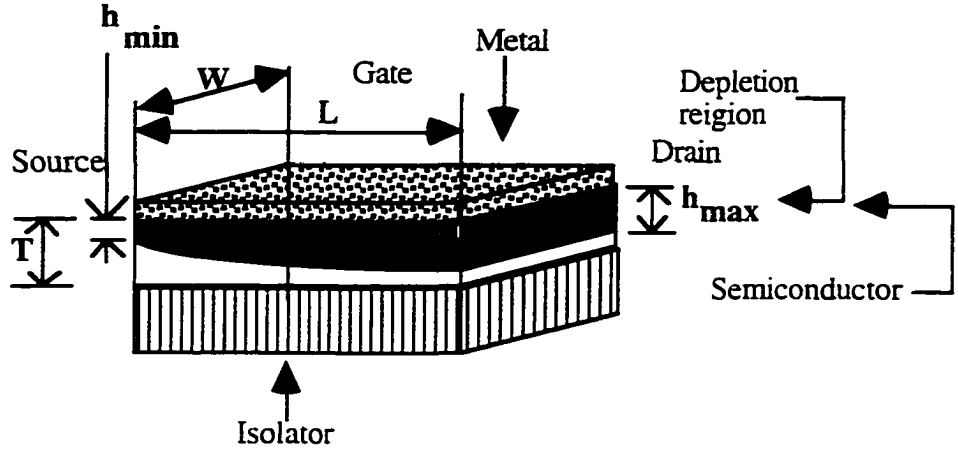

Figure. 1.11. Gate region of a MESFET transistor.

As can be seen from Figure 1.11, a gate metal with length L and width W has been placed on top of a piece semiconductor of thickness T. The height of the depletion region under the gate metal (h) varies along the length of the MESFET. This is due to the fact that the potential of the channel slowly changes from the source voltage (at the source side) to drain

voltage, (at the drain side). Therefore, V_f in the previous equations is the vector addition of the forward gate voltage and V(x), which is the channel potential with respect to the source. As is shown in Figure 1.12. Therefore h(x) can be calculated as:

$$h(x) = \sqrt{\frac{2\varepsilon_S}{qN_B}[\,\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}]} \qquad \text{Eq. 1.29}$$

where V_G is the forward Gate voltage. This means h_{min} could be found at the source side, where V(x) = 0, and the h_{max} could be found at the drain end, where $V(x) = V_D$. That is:

$$h_{min} = \sqrt{\frac{2\varepsilon_S}{qN_B}[\,\Phi_b - V_G - \frac{Kt}{q}]} \quad @ \quad x = 0 \text{ (Source side)} \qquad \text{Eq. 1.30}$$

$$h_{max} = \sqrt{\frac{2\varepsilon_S}{qN_B}[\,\Phi_b - V_G + V_D - \frac{Kt}{q}]} \quad @ \quad x = L \text{ (Drain side)} \qquad \text{Eq. 1.31}$$

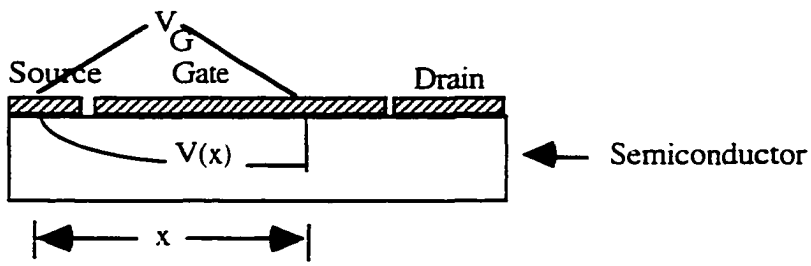

Figure. 1.12. Voltages in a MESFET. V(x) changes with x from the Source to the Drain.

In a practical device the channel thickness, here denoted by upper case T, is limited. Note also that the temperatore is denoted by lower case t. Therefore, the maximum value of h_{max} should be equal or less than T. The point where V_D is large enough to make the h_{max} equal to T is called the "pinch-off point" and this condition is called the "pinch-off condition". The sum of all the relevant voltage contributions for creating this condition is called V_P. Therefore, at the pinch-off point one can write:

$$T = h_{max} = \sqrt{\frac{2\varepsilon_S V_P}{qN_B}} \quad \boxed{\text{Eq. 1.32}}$$

or

$$V_P = \frac{qN_B T^2}{2\varepsilon_S} \quad \boxed{\text{Eq. 1.33}}$$

The current that passes through the device is another important parameter in any electronic device. One way to calculate this parameter in this device is through current density (J_x). It is well known that the current density (J_x) is a function of electric field (E_x) in a linear semiconductor device. This relation is given as:

$$J_x = \sigma_{(x)} E_x \quad \boxed{\text{Eq. 1.34}}$$

Moreover, in a semiconductor $\sigma_{(x)}$ is given as:

$$\sigma_{(x)} = \frac{1}{\rho_{(x)}} = qN_B\mu(x,E) \quad \boxed{\text{Eq. 1.35}}$$

Where μ is the mobility of the majority carriers. Although, carrier's mobility in general is a function of electric field, crystallographic uniformity, and doping concentration; it is assumed that all these factors are constant throughout the channel. In another words it is assumed that the dependence of the mobility to these factors are negligible with in the channel. Therefore, one can write:

$$J_x = qN_B\mu E_x \quad \boxed{\text{Eq. 1.36}}$$

Here, N_B is the concentration of dopant and μ is the mobility of the majority carriers. In another words, in a p-type semiconductor $N_B = N_A$ and $\mu = \mu_h$, for n-type semiconductor $N_B = N_D$ and $\mu = \mu_e$. Let's substitute $-\frac{\partial V}{\partial x}$ for its equivalent E_x. Therefore, we have:

$$J_x = qN_B\mu \left(-\frac{\partial V}{\partial x}\right) \quad \boxed{\text{Eq. 1.37}}$$

The current (I_x) can be calculated by multiplying the current density J by the area, so:

$$I_x = J_x A = J_x W (T - h) \quad \boxed{\text{Eq. 1.38}}$$

$\therefore$

$$I_x = I_D = qN_B\mu W(T - h)(- \frac{\partial V}{\partial x}) \quad \boxed{\text{Eq. 1.39}}$$

or

$$I_D \partial x = - qN_B\mu W(T - h) \partial V \quad \boxed{\text{Eq. 1.40}}$$

However, h is already shown to be a function of V. Therefore, let's substitute in the above equation:

$$I_D \partial x = - qN_B\mu W(T - \sqrt{\frac{2\varepsilon_S}{qN_B}[\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}]}) \partial V \quad \boxed{\text{Eq. 1.41}}$$

Now, let's integrate this function from source to drain, ie. x = 0 to x =L. V(x) is defined with reference to the source making V(x) equal to zero at the source ($V(x) \Big|_{x=0} = 0$) and V(x) is equal to V_D at the drain side ($V(x) \Big|_{x=L} = V_D$). As a result it, can be written:

$$\int_0^L I_D \partial x = - \int_0^{V_D} qN_B\mu W (T - \sqrt{\frac{2\varepsilon_S}{qN_B}[\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}]}) \partial V \quad \boxed{\text{Eq. 1.42}}$$

$$I_D L = - qN_B\mu W \int_0^{V_D} (T - \sqrt{\frac{2\varepsilon_S}{qN_B}[\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}]}) \partial V \quad \boxed{\text{Eq. 1.43}}$$

$$I_D L = - qN_B\mu W \left(TV(x) - \sqrt{\frac{2\varepsilon_S}{qN_B}} (\frac{2}{3}) [\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}]^{\frac{3}{2}} \right)_0^{V_D}$$

$$\boxed{\text{Eq. 1.44}}$$

$$I_D = -\frac{qN_B\mu W}{L}\left(TV(x) - \sqrt{\frac{2\varepsilon_S}{qN_B}}\left(\frac{2}{3}\right)\left[\Phi_b - V_G + V_{(x)} - \frac{Kt}{q}\right]^{\frac{3}{2}} \right)_0^{V_D} \quad \text{Eq. 1.45}$$

$$I_D = -\frac{qN_B\mu W}{L}\left\{ TV_D - \sqrt{\frac{2\varepsilon_S}{qN_B}}\left(\frac{2}{3}\right)\left(\left[\Phi_b - V_G + V_D - \frac{Kt}{q}\right]^{\frac{3}{2}} - \left[\Phi_b - V_G - \frac{Kt}{q}\right]^{\frac{3}{2}} \right)\right\}$$

Eq. 1.46

From definition of V_P early on in this section, it can be written:

$$\frac{V_P}{T^2} = \frac{qN_B}{2\varepsilon_S} \Rightarrow \sqrt{\frac{2\varepsilon_S}{qN_B}} = \frac{T}{\sqrt{V_P}} \quad \text{Eq. 1.47}$$

Let's substitute this for the equation for I_D:

$$I_D = -\frac{qN_B\mu W}{L}\left\{ TV_D - \frac{T}{\sqrt{V_P}}\left(\frac{2}{3}\right)\left(\left[\Phi_b - V_G + V_D - \frac{Kt}{q}\right]^{\frac{3}{2}} - \left[\Phi_b - V_G - \frac{Kt}{q}\right]^{\frac{3}{2}} \right)\right\}$$

Eq. 1.48

$$I_D = -\frac{qN_B\mu WTV_P}{3L}\left\{ \frac{3V_D}{V_P} - 2\left(\left[\frac{\Phi_b - V_G + V_D - \frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}} \right)\right\}$$

Eq. 1.49

Let's define the coefficient of this equation as I_P:

$$I_P = \frac{qN_B\mu WT}{3L} V_P \quad \text{Eq. 1.50}$$

If V_P is substituted in the above equation, an equation based on physical dimensions of the device will result:

$$I_P = \frac{qN_B\mu WT}{3L}\left(\frac{qN_BT^2}{2\varepsilon_S}\right) = \frac{q^2N_B^2\mu WT^3}{6\varepsilon_S L} \quad \text{Eq. 1.51}$$

Therefore, I_D can be expressed as:

$$I_D = -I_P \left\{ \frac{3V_D}{V_P} - 2 \left(\left[\frac{\Phi_b - V_G + V_D - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right\} \quad \text{Eq. 1.52}$$

This equation is valid for both types of MESFETs (n-channel and p-channel). However, the direction of the current and V_G is as given in Figure 1.13 (a). However, it is more logical from circuit designer point of view that this equation state the current value in direction shown in Figure 1.13 (b). The current convention on Figure 1.13(b) is the reverse of that in Figure 1.13(a), creating an equation corresponding to Figure 1.13(b):

$$I_D = I_P \left\{ \frac{3V_D}{V_P} - 2 \left(\left[\frac{\Phi_b - V_G + V_D - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right\} \quad \text{Eq. 1.53}$$

Nevertheless, the current can not increase indefinitely; the saturation current occurs when $\left(\Phi_b - V_G + V_D - \frac{Kt}{q} \right)$ exceed pinch-off voltage (V_P). In another words, the saturation current occurs when the channel is pinched-off.[4] Therefore, it can be written:

$$V_P = \Phi_b - V_G + V_D - \frac{Kt}{q} \quad \text{Eq. 1.54}$$

or

$$V_D = V_P + V_G + \frac{Kt}{q} - \Phi_b \quad \text{Eq. 1.55}$$

Let's substitute this value, in the above equation for I_D to find I_{Dsat}:

$$I_{DSat} = I_p \left\{ \frac{3(V_P + V_G + \frac{KT}{q} - \Phi_b)}{V_P} - 2 \left(\left[\frac{V_P + \phi_b - V_G + V_G + \frac{KT}{q} - \phi_b - \frac{KT}{q}}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\phi_b - V_G - \frac{KT}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right.$$

Eq. 1.56

$$I_{Dsat} = I_P \left\{ 3 \left(\frac{V_P}{V_P} + \frac{V_G + \frac{Kt}{q} - \Phi_b}{V_P} \right) - 2 \left(\left[\frac{V_P}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right\} \quad \text{Eq. 1.57}$$

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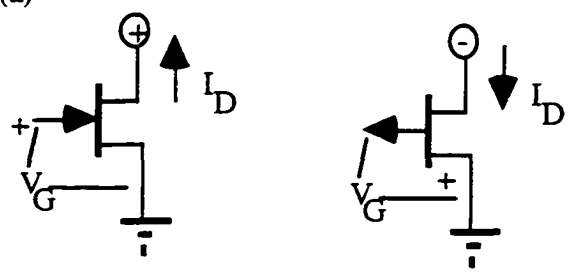
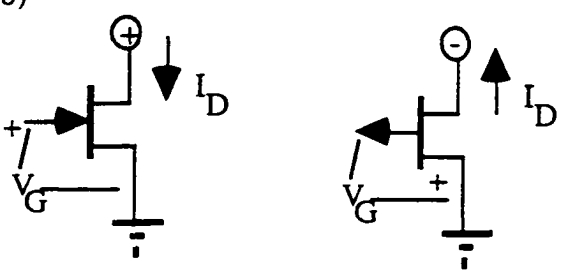
[4] This is a good approximation for most cases. Exact solution requires application of numerical techniques.

(a)



$$I_D = -I_P \left\{ \frac{3V_D}{V_P} - 2 \left(\left[\frac{\Phi_b - V_G + V_D - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right\}$$

(b)



$$I_D = I_P \left\{ \frac{3V_D}{V_P} - 2 \left(\left[\frac{\Phi_b - V_G + V_D - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} - \left[\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right]^{\frac{3}{2}} \right) \right\}$$

Fig. 1.13. Correct current directions and voltage polarizations should be used for the given equation. Figure (a) is more convenient for analytical purposes. Figure (b) is more convenient for circuit designers.

$$I_{Dsat} = I_P \left\{ 1 - 3 \left(\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right) + 2 \left(\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right)^{\frac{3}{2}} \right\} \quad \boxed{\text{Eq. 1.58}}$$

At this juncture all the elements are present to calculate various transconductances, such as $g_m = \frac{\partial I_D}{\partial V_G}$, $g_d = \frac{\partial I_D}{\partial V_D}$ for the case of saturated and unsaturated drain currents. First, let us consider these transconductances for an unsaturated case:

$$g_m=\frac{\partial}{\partial V_G}\left(I_P\left\{\frac{3V_D}{V_P}-2\left(\left[\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}}-\left[\frac{\Phi_b-V_G-\frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}}\right)\right\}\right) \quad \text{Eq. 1.59}$$

$$g_m=\frac{I_P}{V_P}\left\{3\sqrt{\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}}-3\sqrt{\frac{\Phi_b-V_G-\frac{Kt}{q}}{V_P}}\right\} \quad \text{Eq. 1.60}$$

$$g_m=3\frac{I_P}{V_P}\left\{\sqrt{\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}}-\sqrt{\frac{\Phi_b-V_G-\frac{Kt}{q}}{V_P}}\right\} \quad \text{Eq. 1.61}$$

and similarly:

$$g_d=\frac{\partial}{\partial V_D}\left(I_P\left\{\frac{3V_D}{V_P}-2\left(\left[\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}}-\left[\frac{\Phi_b-V_G-\frac{Kt}{q}}{V_P}\right]^{\frac{3}{2}}\right)\right\}\right) \quad \text{Eq. 1.62}$$

$$g_d=3\frac{I_P}{V_P}\left\{1-\sqrt{\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}}\right\} \quad \text{Eq. 1.63}$$

If g_{max} is defined to be:

$$g_{max}=3\frac{I_P}{V_P} \quad \text{Eq. 1.64}$$

Therefore, g_m and g_d can be expressed as:

$$g_m=g_{max}\left\{\sqrt{\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}}-\sqrt{\frac{\Phi_b-V_G-\frac{Kt}{q}}{V_P}}\right\} \quad \text{Eq. 1.65}$$

$$g_d=g_{max}\left\{1-\sqrt{\frac{\Phi_b-V_G+V_D-\frac{Kt}{q}}{V_P}}\right\} \quad \text{Eq. 1.66}$$

Similar calculations can be made for a saturated case:

$$g_{msat} = \frac{\partial I_{Dsat}}{\partial V_G} \quad \text{Eq. 1.67}$$

$$g_{msat} = \frac{\partial}{\partial V_G}\left(I_P \left\{ 1 - 3\left(\frac{\Phi_b - V_G - \frac{Kt}{q} - \Phi_b}{V_P} \right) + 2\left(\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right)^{\frac{3}{2}} \right\} \right)$$

Eq. 1.68

$$g_{msat} = 3\frac{I_P}{V_G}\left\{ 1 - \sqrt{\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P}} \right\} \quad \text{Eq. 1.69}$$

$$g_{msat} = g_{max}\left\{ 1 - \sqrt{\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P}} \right\} \quad \text{Eq. 1.70}$$

As one would expect that g_{dsat} is calculated to be:

$$g_{dsat} = \frac{\partial I_{Dsat}}{\partial V_D} \quad \text{Eq. 1.71}$$

$$g_{dsat} = \frac{\partial}{\partial V_D}\left(I_P \left\{ 1 - 3\left(\frac{\Phi_b - V_G - \frac{Kt}{q} - \Phi_b}{V_P} \right) + 2\left(\frac{\Phi_b - V_G - \frac{Kt}{q}}{V_P} \right)^{\frac{3}{2}} \right\} \right)$$

Eq. 1.72

$$g_{dsat} = 0 \quad \text{Eq. 1.73}$$

2. IMPORTANT DETAILS IN 3DI TECHNOLOGY

A detailed consideration of several other points are necessary before an attempt to develop a practical 3DI technology can be made. The other significant adversities faced with when pursuing a 3DI technology, as well as their prospective solutions, are the subjects of study in this chapter.

2.1. Cross-Talk in 3DI Technology

One of the most troubling predicaments of a 3DI technology is cross-talk.[13] The problem of cross-talk is direct result of close proximity of the layers in 3DI technology. The wires in closely packed layers act as capacitors and pass AC signals from one layer to the other layer. Moreover, the electromagnetic disturbance of the space that surrounds a layer from current fluctuations in that layer, induces current in the adjacent layers. Of course, as one might expect, this problem worsens in higher frequencies. This relationship is rooted in the fact that the higher the frequency, the lower the impedance of the capacitance between the layers and the better the electromagnetic coupling between the layers.

The currents and potentials, induced as result of cross-talk, may create false logical states. For example, if the cross-talk occurs on the clock lines, then the devices connected to that clock line might trigger at a wrong time, causing a logic error in the circuit. Fig. 2.1 presents a cross-talk coupling between two adjacent layers.[13]

To better understand this phenomenon, consider two tightly spaced parallel signal lines in two adjacent layers. These lines could be made of metal conductors, polysilicon lines, or any other conductive material in the signal path. The voltage change in one of these lines disturbs the tranquillity of electric and magnetic fields in the space around it. This disturbance to the tranquillity of electric and magnetic field induces a voltage and a current on the other line. This interdependence between these two lines can be modeled as shown in Fig. 2.2.[14]

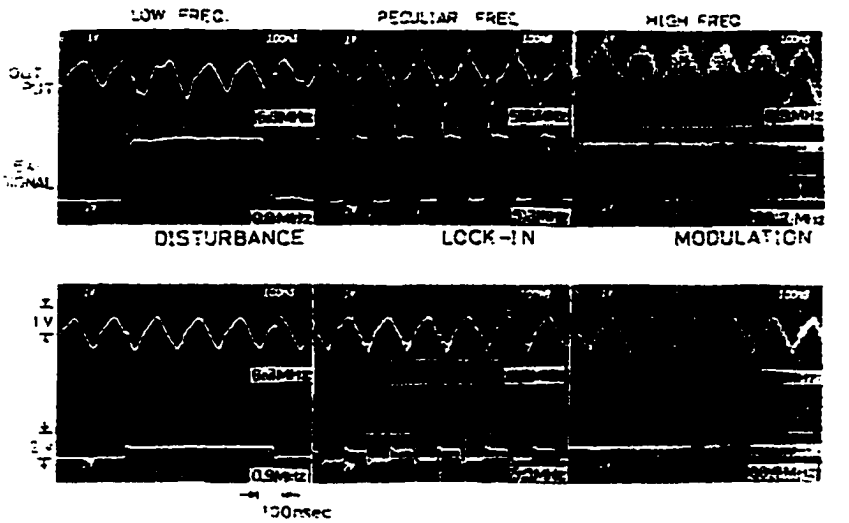


Fig. 2.1. Dependence of the wave form of the ring oscillator in second layer on the external signal given from underlying active layer.[13]

It can be observed in Fig. 2.2 that cross talk creates two sources of currents on the second line. The first one is the current through capacitor C_m , denoted by i_C , and second one is due to presence of mutual inductance, i_L. The capacitor in this model is the mutual capacitance that forms in-between two layers. The mutual inductor is formed from that the length of the line that is exposed to magnetic flux of the other line.

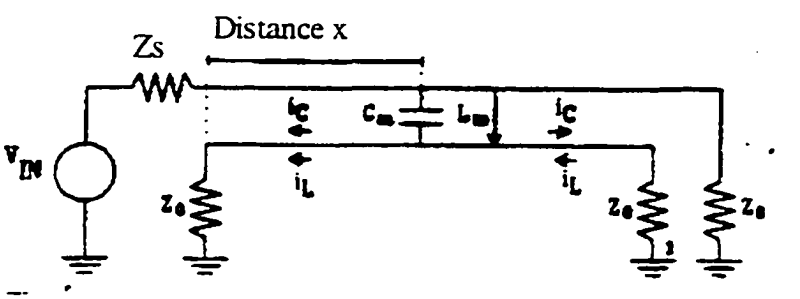


Fig. 2.2. A model for analyzing the cross-talk.[14]

A more scientific way to analyze the cross-talk phenomenon is through coupled transmission lines. An ideal coupled transmission line is presented in Fig. 2.3. An excellent analysis of such transmission line is presented by Post et al.[15] However, here the objective is to eliminate this problem, not to analyze it. A technique to eliminate this problem is discussed in the following section.

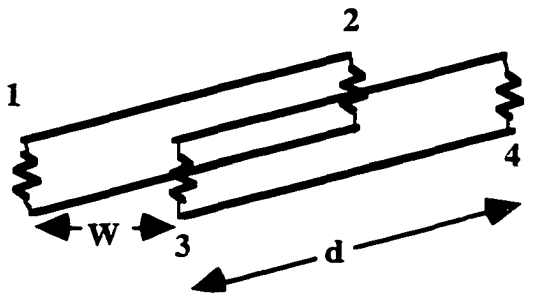


Fig. 2.3. A Classical coupled transmission line.

2.1.1. Inter-Layer Shield

As mentioned in the previous section, one of the problems associated with 3DI technology is the problem of cross-talk. It was also noted that the adjacent layers can be viewed as a coupled transmission lines. To better grasp this concept let us investigate Fig. 2.4.

It can be seen from the equivalent circuit of Fig. 2.4.B that there is mutual inductance, modeled as a transformer, and mutual capacitance between the two layers. Of course, the conductance G is usually small enough that it can be ignored in any relevant calculation for most practical purposes. The mutual inductance is due to the magnetic flux density leakage, which is created by one line. The change in the magnetic flux can induce an electromagnetic force on the other line. Whereas, the mutual capacitance between these two line results from electric flux density there. The electrical and magnetic coupling between the two layers are demonstrated in Fig. 2.5.

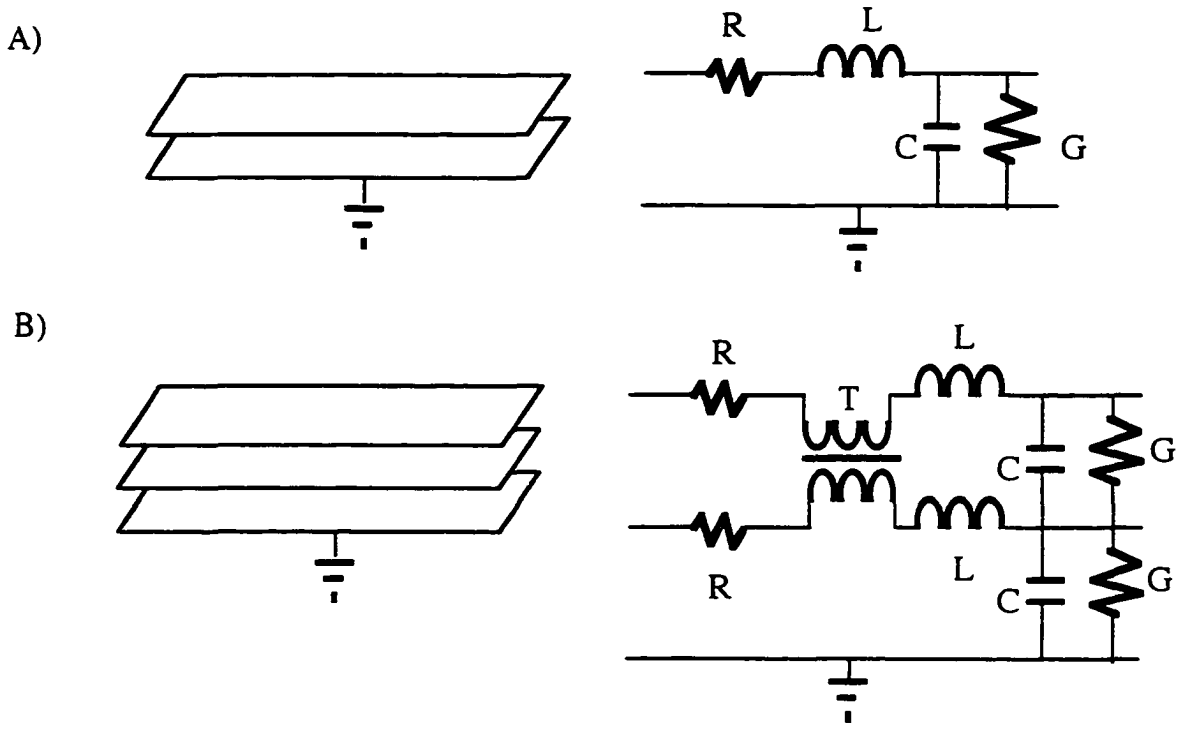


Fig. 2.4. The equivalent circuits of (a) a signal layer and (b) two closely packed layers.

Even though, the exact analysis of these fields is a laborious job and for almost all practical purposes computer simulation is needed; the exact value of these fields are of little use to this study. It is sufficient to note that the mutual capacitance between the layers increases with the area of these elements and decreases with the distance in-between them. A rough estimate of this mutual capacitance can be calculated using capacitance formula:

$$C = K\frac{A}{d} \qquad \text{Eq. 2.1}$$

Similarly, the mutual inductance between the lines is related to the length of these lines and inversely related their distance from each other. Therefore, one way to decrease the cross-talk problem is to decrease the length of these lines, or to increase the distance between them. However, in most cases it is not practical either to decrease the length of these transmission lines, or to increase the distance between them.

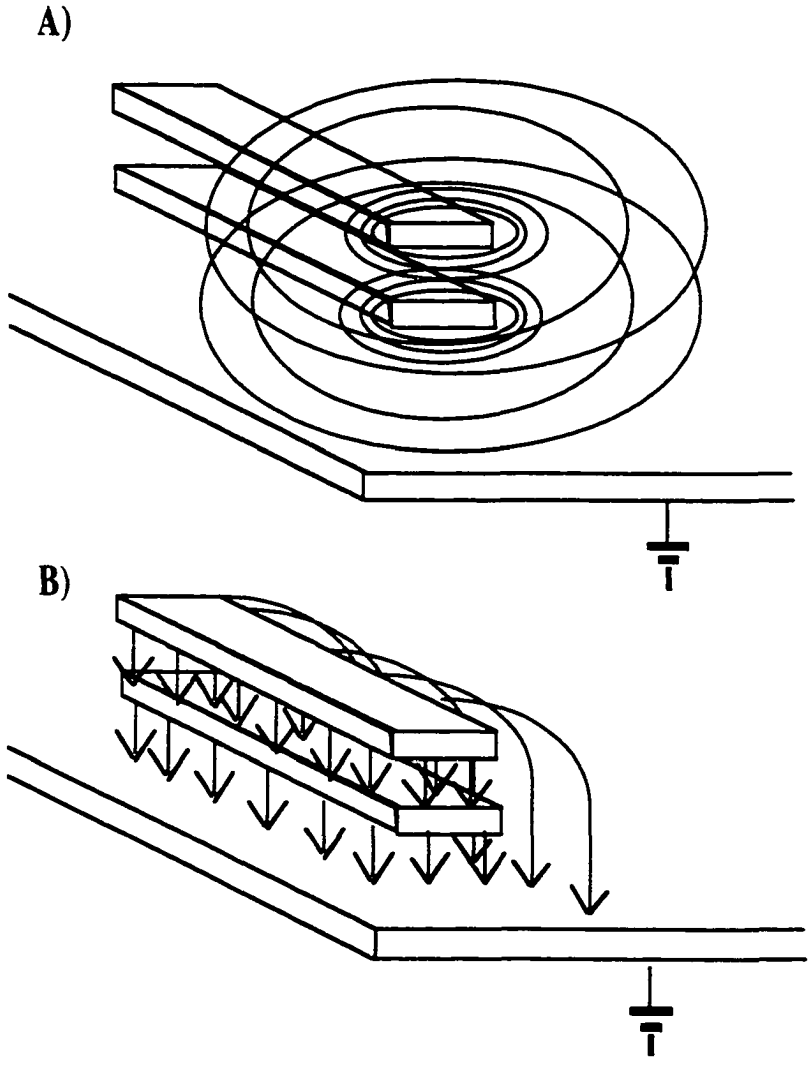


Fig. 2.5. The magnetic (a) and the electric (b) flux of two closely stacked layers.

The solution suggested in this paper is to shield these two layers by placing a ground layer in-between them. As shown in Fig. 2.6. The ground layer placed in-between the two layers can be called a shield. It will be shown in the next section that this shield layer, if designed properly, can almost eliminate the electromagnetic interaction between the layers. Therefore, this will reduce the problem of cross-talk to an acceptable level. In the next section, it will be shown analytically how well a shield layer eliminates the problem of cross-talk.

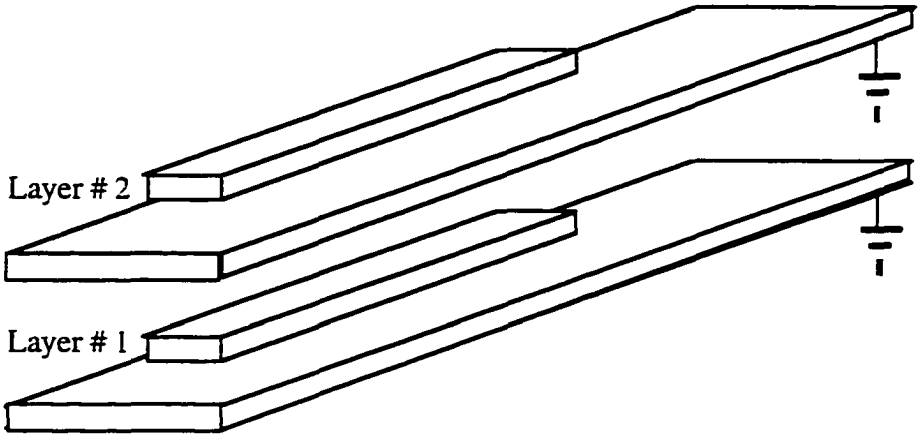


Fig. 2.6. Inter-Layer Shields are grounded in order to eliminate the problem of cross-talk.

It is known that the best electromagnetic shields are the best conductors, such as metals. However, due to the fact that it is extremely hard to grow semiconductor materials on top of metals, one might use other conducting materials, such as polysilicon or other forms of degenerate semiconductors. Moreover, it is also possible to use the ion implantation technique to place a metal layer underneath a semiconductor layer. This technique enables one to grow insulator first. Then using the ion implant technique, one can implant a metallic surface in middle of the insulator layer.

2.1.1.1. A Theoretical Analysis of the Inter-Layer Shield

In the previous section it was suggested that the use of a correctly designed conductive shields can eliminate the problem of cross-talk. In this section, it will be demonstrated analytically that this is indeed the case. That is, it will be established that the electromagnetic radiation generated as result of the current disturbance in one line will not, for most part, pass through this shield.

To start our analysis, let's consider a TEM electromagnetic wave propagating through a lossy dielectric material.[15] Therefore:

$$\nabla \times E = -j\omega\mu H \qquad \text{Eq. 2.2}$$

$$\nabla \times H = j\omega\varepsilon E + \sigma E \qquad \text{Eq. 2.3}$$

$$\nabla \times H = j\omega\left(\varepsilon + \frac{\sigma}{j\omega}\right) E \qquad \text{Eq. 2.4}$$

$$\nabla \times H = j\omega\varepsilon_0\left(\varepsilon_r - \frac{j\sigma}{\omega\varepsilon_0}\right) E \qquad \text{Eq. 2.5}$$

$$\nabla \times H = j\omega\varepsilon_0 \varepsilon' E \qquad \text{Eq. 2.6}$$

Now substituting the first equation in the this equation, it can be written:

$$\nabla \times \left(\frac{\nabla \times E}{-j\omega\mu}\right) = j\omega\varepsilon_0 \varepsilon' E \qquad \text{Eq. 2.7}$$

$$\nabla \times (\nabla \times E) = \omega^2\varepsilon_0 \varepsilon'\mu E \qquad \text{Eq. 2.8}$$

$$\nabla(\nabla . E) - \nabla^2 E = \omega^2\varepsilon_0 \varepsilon'\mu E \qquad \text{Eq. 2.9}$$

$$\nabla\left(\frac{\rho}{\varepsilon_0 \varepsilon_r}\right) - \nabla^2 E = \omega^2\varepsilon_0 \varepsilon'\mu E \qquad \text{Eq. 2.10}$$

Assuming that the charge density is constant through out the shield region, that is $\rho_{(x,y,z)}$ = Constant, it can be written:

$$-\nabla^2 E = \omega^2 \varepsilon_0 \varepsilon' \mu E \quad \text{Eq. 2.11}$$

This is the famous wave equation and the solution is known to be:

$$E = a e^{\gamma Z} + b e^{-\gamma Z} \quad \text{Eq. 2.12}$$

where:

$$\gamma = j\omega\sqrt{\mu\, \varepsilon_0\, \varepsilon'} \quad \text{Eq. 2.13}$$

$$\gamma = j\omega\sqrt{\mu\varepsilon_0\left(\varepsilon_r - \frac{j\sigma}{\omega\varepsilon_0}\right)} = j\omega\sqrt{\mu\varepsilon\left(1 - \frac{j\sigma}{\omega\varepsilon}\right)} = \sqrt{j\omega\mu\,(\sigma + j\omega\varepsilon)} = \alpha + j\beta \quad \text{Eq. 2.14}$$

This equation correctly determines γ for all the practical cases with real μ. However, in this study the interest is to investigate the penetration of the electromagnetic waves into the shield. Moreover, this shield is usually made of highly conductive materials. This means the term $(\frac{j\sigma}{\omega\varepsilon})$ in the above equation is much larger than one. So, it can be written:

$$\gamma = j\omega\sqrt{\mu\varepsilon\left(1 - \frac{j\sigma}{\omega\varepsilon}\right)} \approx j\omega\sqrt{\mu\varepsilon\left(-\frac{j\sigma}{\omega\varepsilon}\right)} = \sqrt{\frac{\omega\mu\sigma}{2}} + j\sqrt{\frac{\omega\mu\sigma}{2}} \quad \text{Eq. 2.15}$$

Therefore, α and β can be written as:

$$\alpha = \beta = \sqrt{\frac{\omega\mu\sigma}{2}} \quad \text{Eq. 2.16}$$

As can be seen from the wave equation, α is responsible for the decay in the wave amplitude. Moreover, it can also be seen from the above formula that α is related to the square root of frequency. That is, the electromagnetic waves with higher frequencies decay faster than the electromagnetic waves with lower frequencies. To better demonstrate this, let's define the

depth of penetration (δ) to be the distance of a point where the amplitude of the wave has fallen to ($\frac{1}{e}$) of its amplitude at the surface of the shield. Therefore, it can be written:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad \text{Eq. 2.17}$$

Now, let's consider a few examples of practical shield materials with infinite thickness. Let's further presume that the μ is equal to μ_o(4π X 10^{-9} $\frac{H}{cm}$). Therefore, the penetration depth can be calculated for different frequencies using the above formula. The results of these calculations, for several frequencies, has been tabulated in Table. 2.1. Moreover, in Fig 2.7 the penetration depth vs. frequency for different values of resistivities are plotted.

Table 2.1. Penetration depth at different frequencies for different resistivity materials. First five columns n-type silicon with doping densities of 4.5e13 cm^{-3} (ρ = 100 Ω–cm), 4.5e14 cm^{-3} (ρ= 10 Ω–cm), 4.5e15 cm^{-3} (ρ = 1 Ω–cm), 6.5e16 cm^{-3} (ρ = 0.1 Ω–cm), 4.5 e18 cm^{-3} (ρ = 0.01 Ω–cm) and the last column copper.

	ρ = 100 (Ω–cm)	ρ = 10 (Ω–cm)	ρ = 1 (Ω–cm)	ρ = 0.1 (Ω–cm)	ρ = 0.01 (Ω–cm)	1.68×10^{-6} (Ω–cm)
10 KHz	5.03 (m)	1.59 (m)	0.503 (m)	0.159 (m)	5.03 (cm)	661 (μm)
100 KHz	1.59 (m)	0.503 (m)	0.159 (m)	5.03 (cm)	1.59 (cm)	208. (μm)
1 MHz	0.503 (m)	0.159 (m)	5.03 (cm)	1.59 (cm)	5032 (μm)	66.1 (μm)
10 MHz	0.159 (m)	5.03 (cm)	1.59 (cm)	5032 (μm)	1591 (μm)	20.8 (μm)
100 MHz	5.03 (cm)	1.59 (cm)	5032 (μm)	1591 (μm)	503 (μm)	6.61 (μm)
1 GHz	1.59 (cm)	5032 (μm)	1591 (μm)	503 (μm)	159 (μm)	2.08 (μm)

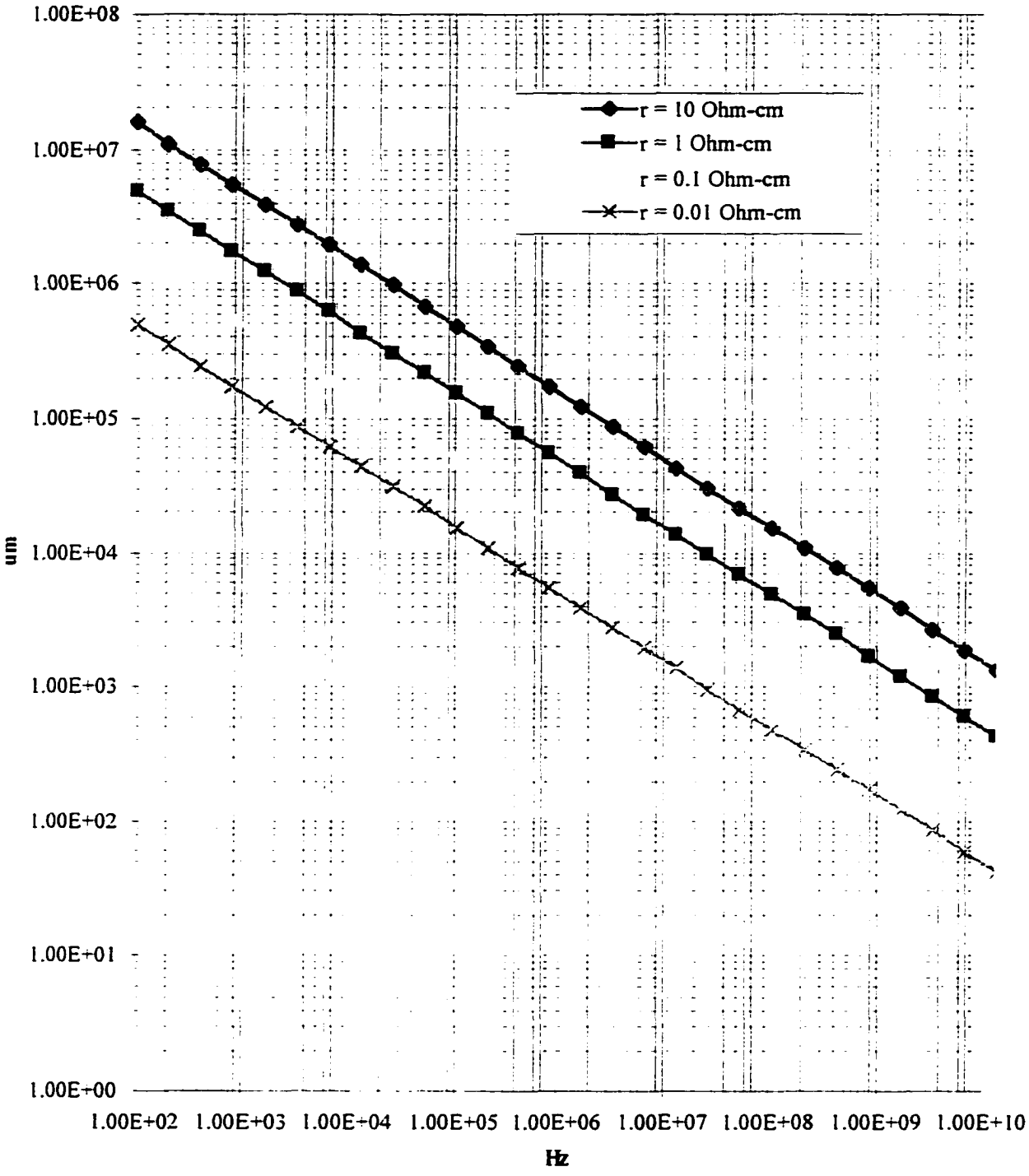


Fig. 2.7. Depth of penetration vs. frequencies for different resistivity materials.

Furthermore, Eq. 2.2 of this chapter states that:

$$\nabla \times E = -j\omega\mu H \qquad \text{Eq. 2.18}$$

Using Eq. 2. 12, assuming the E is in x direction and moving in z direction, it can be written:

$$\nabla \times (a\, e^{+\gamma Z} + b\, e^{-\gamma Z})\, \hat{x} = -j\omega\mu H \qquad \text{Eq. 2.19}$$

$$\begin{vmatrix} \hat{x} & \hat{y} & \hat{z} \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \frac{\partial}{\partial z} \\ (a\, e^{+\gamma Z} + b\, e^{-\gamma Z}) & 0 & 0 \end{vmatrix} = -j\omega\mu H \qquad \text{Eq. 2.20}$$

$$(a\gamma e^{+\gamma Z} - b\gamma e^{-\gamma Z})\, \hat{y} = -j\omega\mu H \qquad \text{Eq. 2.21}$$

$$(-a\gamma e^{+\gamma Z} + b\gamma e^{-\gamma Z})\, \hat{y} = +j\omega\mu H \qquad \text{Eq. 2.22}$$

$$H = \left(\frac{-a\gamma}{j\omega\mu} e^{+\gamma Z} + \frac{b\gamma}{j\omega\mu} e^{-\gamma Z}\right) \hat{y} \qquad \text{Eq. 2.23}$$

This means, there are two waves: one traveling in positive Z direction and the other one moving in the negative Z direction. Therefore, the intrinsic impedance can be calculated as:

$$\eta = \frac{E}{H} = \frac{a\, e^{+\gamma Z}}{-\frac{-a\gamma}{j\omega\mu} e^{+\gamma Z}} = \frac{b\, e^{-\gamma Z}}{\frac{b\gamma}{j\omega\mu} e^{-\gamma Z}} \qquad \text{Eq. 2.24}$$

$$\eta = \frac{j\omega\mu}{\gamma} = j\omega\mu\gamma^{-1} \qquad \text{Eq. 2.25}$$

Substituting for γ from Eq. 2.14 results:

$$\eta = \frac{j\omega\mu}{j\omega\sqrt{\mu\varepsilon\left(1 - \frac{j\sigma}{\omega\varepsilon}\right)}} = \sqrt{\frac{\mu}{\varepsilon\left(1 - \frac{j\sigma}{\omega\varepsilon}\right)}} = \sqrt{\frac{j\omega\mu}{\sigma + j\omega\varepsilon}} \qquad \text{Eq.2.26}$$

For fairly good conductors $\frac{\sigma}{\omega\varepsilon} >> 1$. Therefore:

$$\eta_{\text{good conductors}} \approx \sqrt{\frac{\omega\mu}{\sigma}}\, j \qquad \text{Eq. 2.27}$$

$$\eta_{\text{good conductors}} \approx \sqrt{\frac{\omega\mu}{\sigma}}\, e^{j(+45)} = \sqrt{\frac{\omega\mu}{2\sigma}} + j\sqrt{\frac{\omega\mu}{2\sigma}} \qquad \text{Eq. 2.28}$$

Similarly, for non-conductive materials, such as SiO_2, η could be calculated from Eq. 2.26, and the fact that $\sigma \approx 0$; therefore:

$$\eta_{\text{non-conductive}} = \frac{\mu}{\sqrt{\mu\varepsilon}} = \sqrt{\frac{\mu}{\varepsilon}} \qquad \text{Eq. 2.29}$$

As can be seen in Fig. 2.8, an electromagnetic wave generated at one side of the shield has to overcome three main roadblocks in order to make it to the other side. The first barrier is the interface between the insulator and the shield in one side of the shield. This interface causes part of the wave to be reflected. Next, the wave goes through attenuation inside the shield and another part of it will be reflected from the interface on the other side of the shield. In a similar fashion, the wave under goes several reflections, while being attenuated in side the shield. Fig. 2.8 demonstrates this phenomenon.

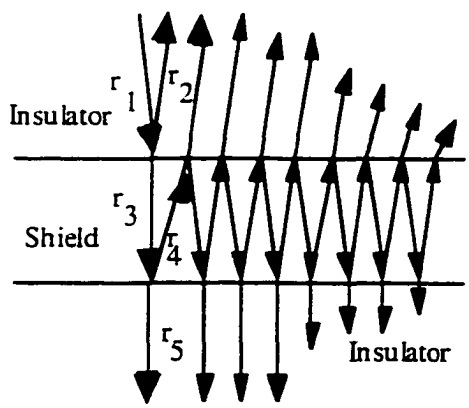


Fig. 2.8. The incident wave on the shield undergoes several reflections and attenuates inside the shield.

To account for this multiple reflections let us reinstate wave equations (Eq. 2.11) for E and H fields in the shield region, as shown in Fig. 2.9:

$$E_{(Z)} = E_o^+ e^{-\gamma Z} + E_o^- e^{+\gamma Z}$$
$$H_{(z)} = H_o^+ e^{-\gamma Z} + H_o^- e^{+\gamma Z} \qquad \text{Eq. 2.30}$$

It is obvious from Fig 2.9 that:

$$\frac{E_i}{H_i} = \frac{-E_r}{H_r} = \eta_1 \qquad \text{Eq. 2.31}$$

$$\frac{E^+}{H^+} = \frac{-E^-}{H^-} = \eta_2 \qquad \text{Eq. 2.32}$$

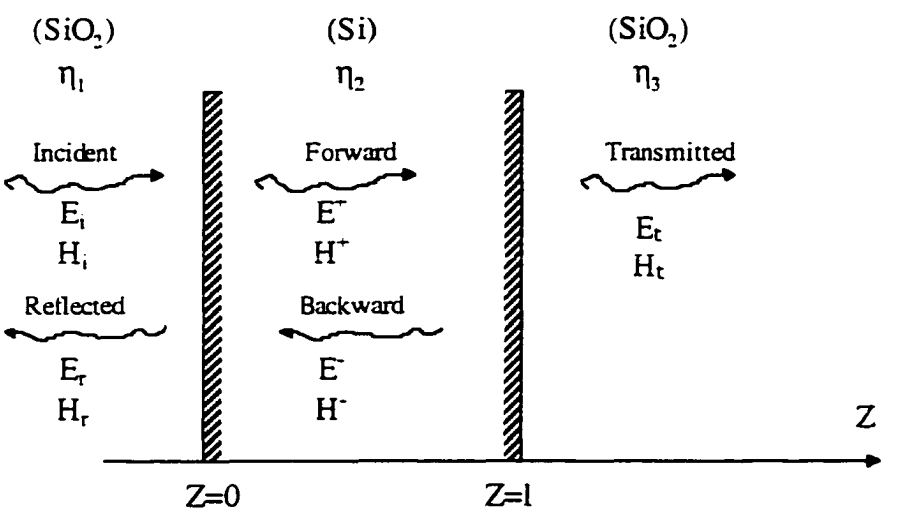


Fig. 2.9. The Electromagnetic waves and corresponding fields in a slab-configuration utilized as shield in between the layers of semiconductor.

$$\frac{E_t}{H_t} = \eta_3 \quad \text{Eq. 2.33}$$

Let us also define reflection and transmission coefficient as follows:

$$\Gamma = \frac{E_r}{E_i} \quad \text{Eq. 2.34}$$

$$t = \frac{E_t}{E_i} \quad \text{Eq. 2.35}$$

The tangential components of electric and magnetic fields must be continuous (there is no current on the surface of the boundary); therefore, at Z=0 Eq. 2.30 can be written as:

$$E_i + E_r = E_o^+ + E_o^-$$
$$\frac{E_i}{\eta_1} - \frac{E_r}{\eta_1} = \frac{E_o^+}{\eta_2} - \frac{E_o^-}{\eta_2} \quad \text{Eq. 2.36}$$

Utilizing Eqs. 2.31 to 2.34 the above can be expressed in terms of reflection coefficient and the intrinsic impedance of the materials involved:

$$(1+\Gamma)E_i = E_o^+ + E_o^-$$
$$\frac{\eta_2}{\eta_1}(1-\Gamma)E_i = E_o^+ - E_o^- \quad \text{Eq. 2.37}$$

These equations can be solved for the variable on the right side:

$$E_o^+ = \frac{E_i}{2}\left[(1+\Gamma) + \frac{\eta_2}{\eta_1}(1-\Gamma)\right]$$
$$E_o^- = \frac{E_i}{2}\left[(1+\Gamma) - \frac{\eta_2}{\eta_1}(1-\Gamma)\right] \quad \text{Eq. 2.38}$$

On the other side of the shield the tangential components of the electric and magnetic field must be continuous; therefore, at Z = L it can be written:

$$E_t = E_o^+ e^{-\gamma L} + E_o^- e^{+\gamma L}$$

$$H_t = \frac{1}{\eta_2}\left[E_o^+ e^{-\gamma L} - E_o^- e^{+\gamma L}\right] \quad \text{Eq. 2.39}$$

Substituting Eq. 3.38 into Eq. 3.39 and rearranging the terms yields:

$$E_t = E_i\left[(1+\Gamma)\text{Cosh}(\gamma L) - \frac{\eta_2}{\eta_1}(1-\Gamma)\text{Sinh}(\gamma L)\right]$$

$$H_t = \frac{E_i}{\eta_2}\left[\frac{\eta_2}{\eta_1}(1-\Gamma)\text{Cosh}(\gamma L) - (1+\Gamma)\text{Sinh}(\gamma L)\right] \quad \text{Eq. 2.40}$$

Let's calculate the admittance at other side of shield, Z=L:

$$\frac{E_t}{H_t} = \eta_3 = \frac{E_i\left[(1+\Gamma)\text{Cosh}(\gamma L) - \frac{\eta_2}{\eta_1}(1-\Gamma)\text{Sinh}(\gamma L)\right]}{\frac{E_i}{\eta_2}\left[\frac{\eta_2}{\eta_1}(1-\Gamma)\text{Cosh}(\gamma L) - (1+\Gamma)\text{Sinh}(\gamma L)\right]} \quad \text{Eq. 2.41}$$

Solving the above equation for Γ:

$$\Gamma = \frac{\left(\frac{\eta_3}{\eta_1} - 1\right) + \left(\frac{\eta_2}{\eta_1} - \frac{\eta_3}{\eta_2}\right)Tanh(\gamma L)}{\left(\frac{\eta_3}{\eta_1} + 1\right) + \left(\frac{\eta_2}{\eta_1} + \frac{\eta_3}{\eta_2}\right)Tanh(\gamma L)} \quad \text{Eq. 2.42}$$

This is an important equation that we will use to plot the reflectivity of various shields.

Similarly τ can be calculated from the top part of Eq. 2.40:

$$\tau = \left[(1+\Gamma)\text{Cosh}(\gamma L) - \frac{\eta_2}{\eta_1}(1-\Gamma)\text{Sinh}(\gamma L)\right] \quad \text{Eq. 2.43}$$

Of course, the reflected power (reflectance) can be calculated as:

$$P_{\text{Reflected}} = R = \frac{\left|\Gamma E_i\right|^2}{\eta_1} \quad \text{Eq. 2.44}$$

Similarly, the transmitted power (transmitance) can be written as:

$$P_{transmitted} = T = \frac{|\tau E_i|^2}{\eta_3} \quad \text{Eq. 2.45}$$

Total power absorbed by the shield can be calculated by:

$$A = 1 - (R + T) \quad \text{Eq. 2.46}$$

Equation 2.44 is utilized to plot the reflectance Vs. frequency of shields with various values of resistivities and conductivities in Fig. 2.10 and 2.11. Similarly, equation 2.45 is utilized to plot the transmitance Vs. frequency of shields with various values of resistivities and conductivities in Fig. 2.12 and 2.13. Finally equation 2.46 is employed to plot the absorbed power ratio in the shield Vs. frequency of shields with various values of resistivities and conductivities in Fig. 2.14 and 2.15.

A quick look at the plots outlined here reveals that they are fairly constant for the scope of our analysis. To understand this let us analyze this phenomenon. When $\sigma >> j\omega\varepsilon$ Eq. 2.14 and Eq. 2.26 can be written as:

$$\gamma = \sqrt{j\omega\mu\sigma} \quad \text{Eq. 2.47}$$

$$\eta = \sqrt{\frac{j\omega\mu}{\sigma}} \quad \text{Eq. 2.48}$$

Also, when $\eta_2 << \eta_1 = \eta_3$ and $|\gamma l|$ is almost 0 then Tanh(γl) is almost equal to γl; therefore, Eq. 2.42 can be expressed for this particular case as:

$$\Gamma = \frac{-\eta_1 \sigma L}{2 + \eta_1 \sigma L} \quad \text{Eq. 2.49}$$

As can be observed form the equation above there is no dependence on frequency. Let us take a closer look at one of the required conditions for the validity of the Eq. 2.49, that is $\eta_2 << \eta_1$. Since material one is non-conductive (SiO_2), it can be written:

$$\sqrt{\frac{j\omega\mu}{\sigma}} << \sqrt{\frac{\mu}{\varepsilon_r\varepsilon_o}} \qquad \text{Eq. 2.50}$$

Therefore:

$$\omega << \frac{\sigma}{\varepsilon_{r1}\varepsilon_o} \qquad \text{Eq. 2.51}$$

On the other hand we know that $|\sigma| >> |j\omega\varepsilon|$ therefore:

$$\omega << \frac{\sigma}{\varepsilon_{r2}\varepsilon_o} \qquad \text{Eq. 2.52}$$

These equations suggest that for higher values of the frequency Eq. 2.49 will not be valid. Therefore, the general form (ie. Eq. 2.42 which is frequency dependent) will predict the characteristics of the reflected power. To examine this we plotted the transmitted power for such cases in Figs. 2.16 and 2.17. To achieve such condition we selected thickness to be 2 mm in Fig. 2.16 and conductivity to be 2e+4 Ohm-M in Fig. 2.17.

One could observe from these plots that after the frequency gets close to values predicted by Eq. 2.51 and Eq. 2.52 the curves, which were showing frequency independent characteristics, suddenly exhibits frequency dependent characteristics. This is consistent with our expectations. Another observation that can be made is the fact that the frequency dependent characteristics for fairly conductive materials only occur at very large thickness, in compare to micro-electronics dimensions, or extremely high frequencies. Finally, as it is predicted from Eq. 2.49 these figures indicate the thicker or more conductive the shield is at the frequency of interest, the more reflective it is. This observation is in line with common sense.

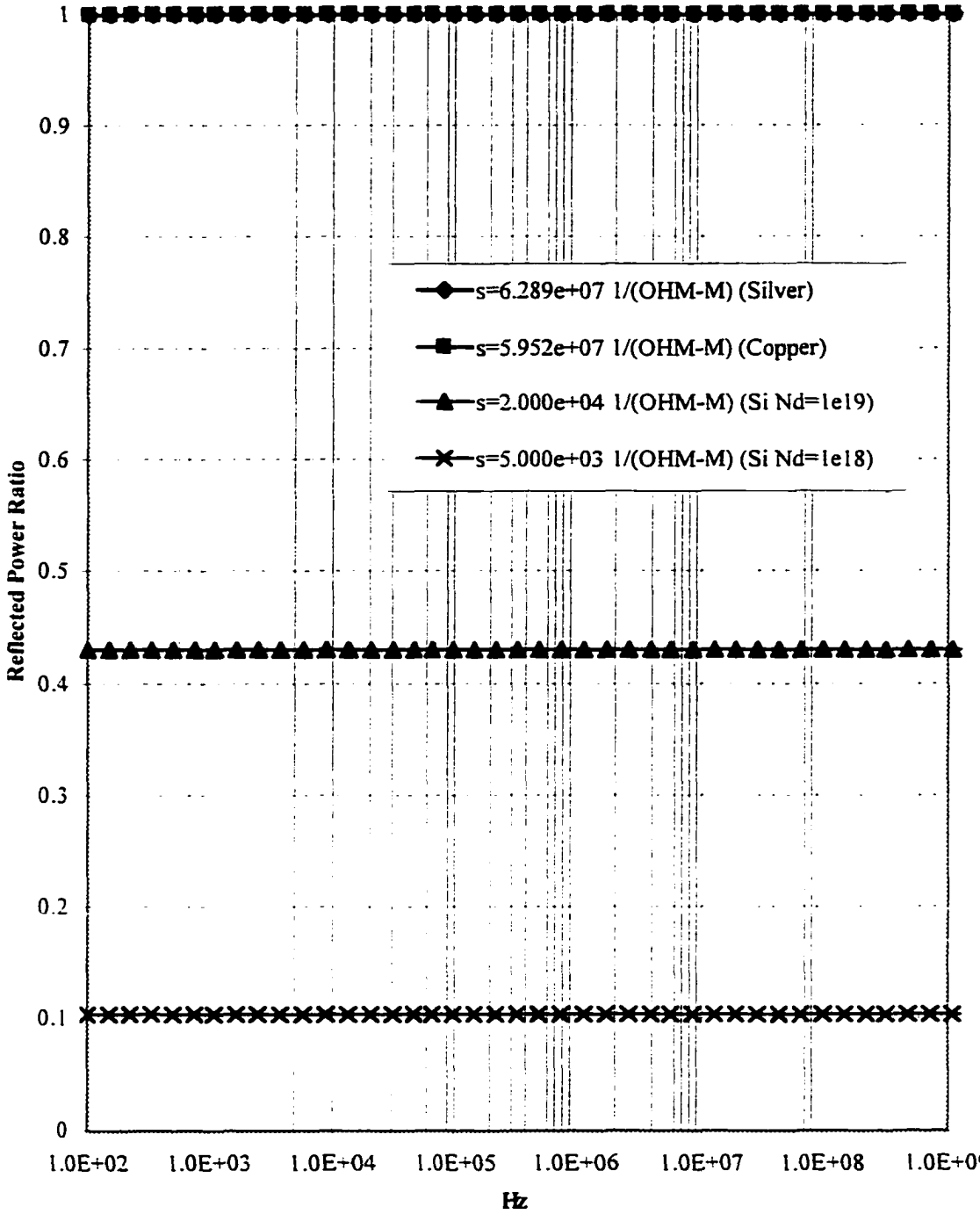


Fig. 2.10 The reflected power ratio vs. frequency for shield with 1 μm thickness and various conductivities, which is placed in the middle SiO_2. In this graph conductivity is designated as s.

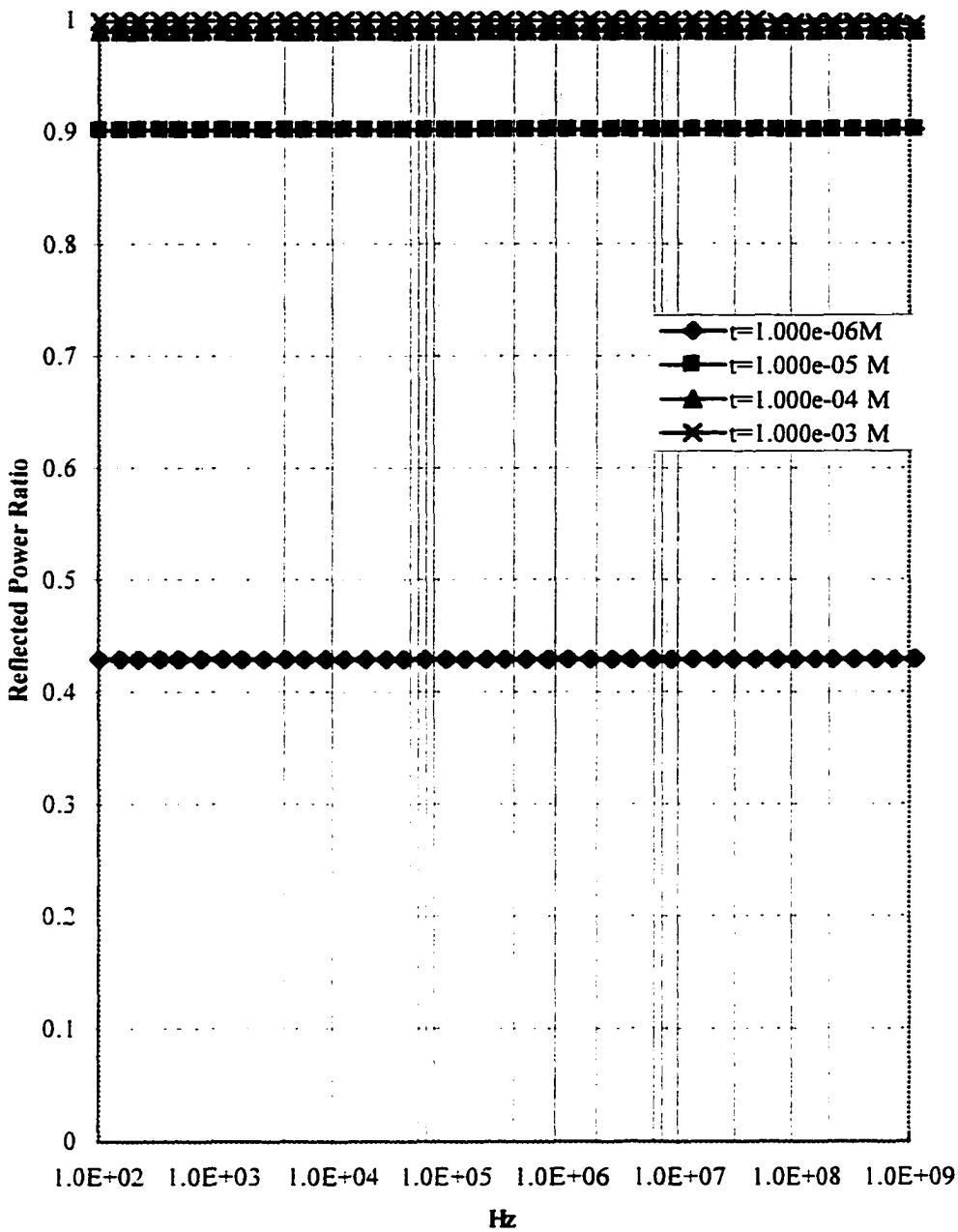


Fig. 2.11 The reflected power ratio vs. frequency for shield with 2E+4 Ohm-M conductivity and various thicknesses, which is placed in the middle SiO_2.

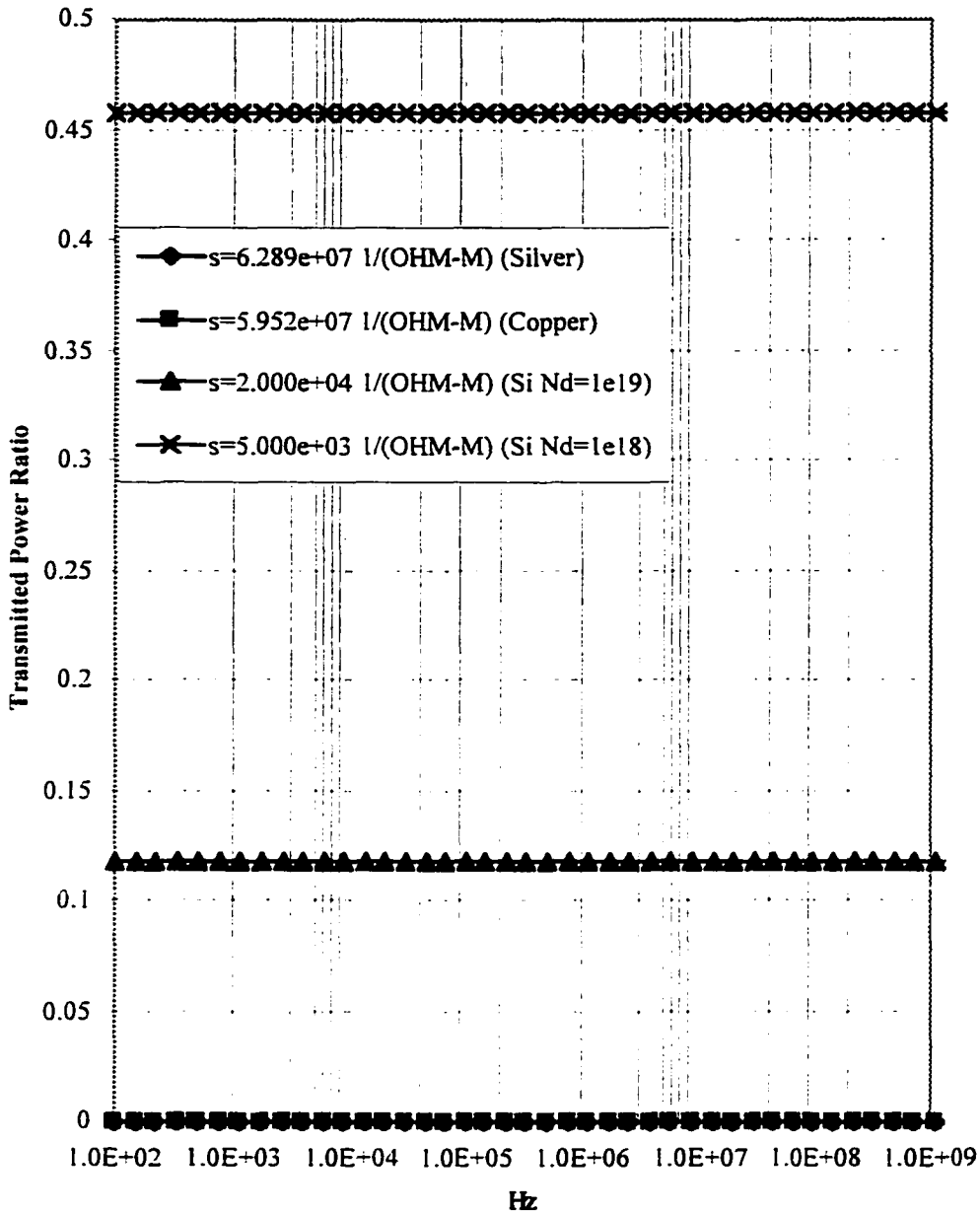


Fig. 2.12 The transmitted power ratio vs. frequency for shield with 1 μm thickness and various conductivities, which is placed in the middle SiO_2. . In this graph conductivity is designated as s.

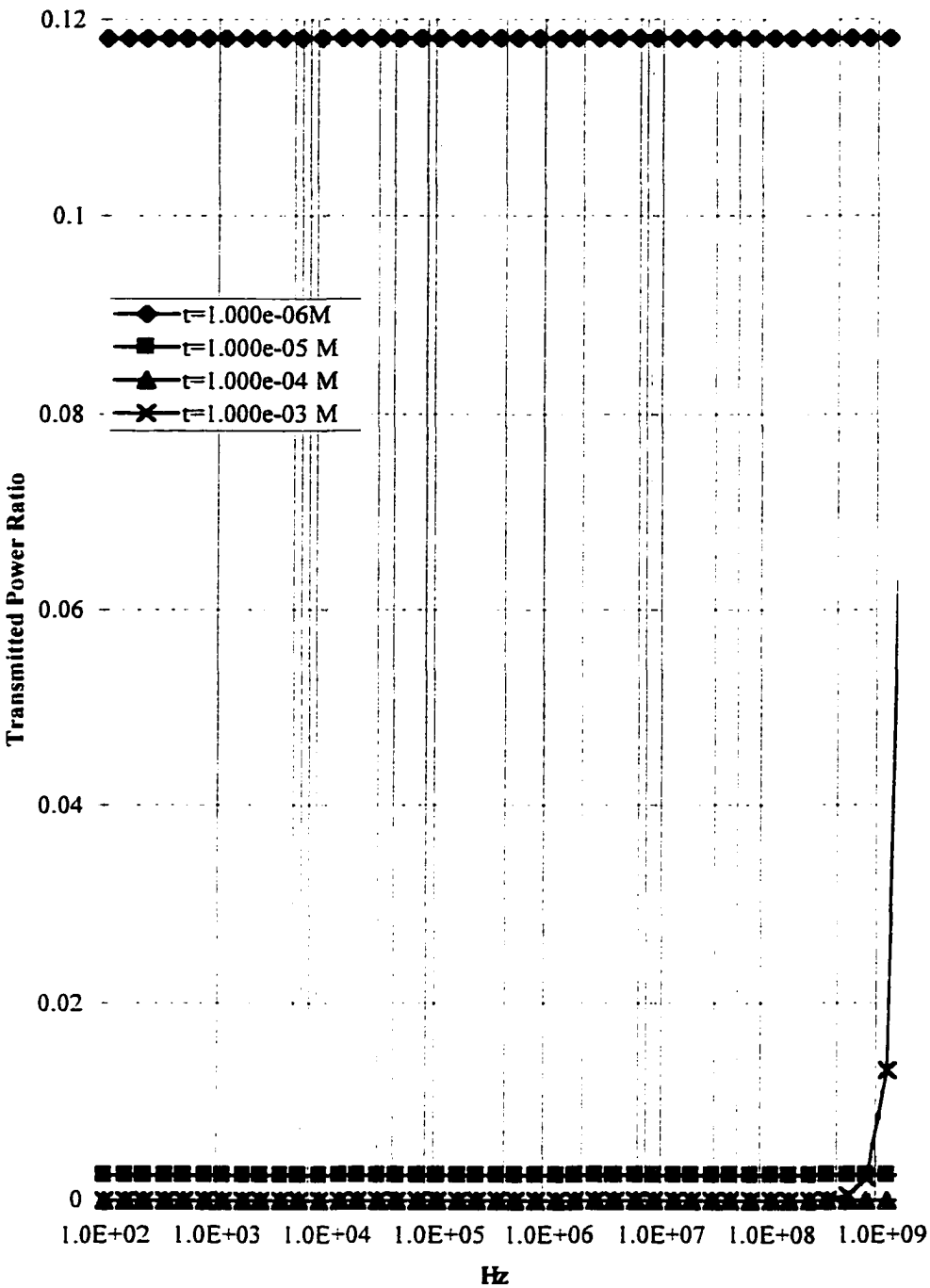


Fig. 2.13 The transmitted power ratio vs. frequency for shield with 2E+4 Ohm-M conductivity and various thicknesses, which is placed in the middle SiO_2.

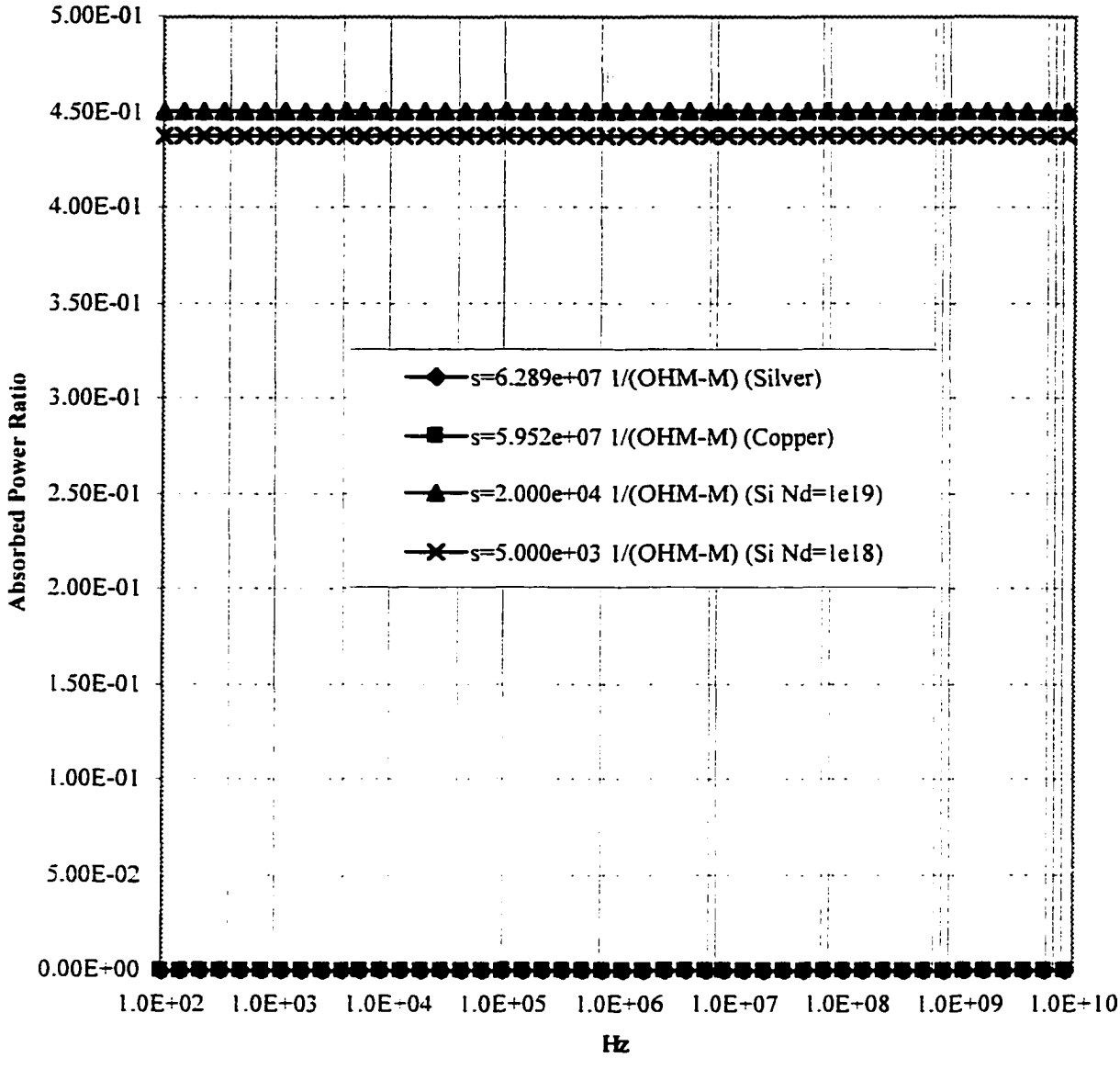


Fig. 2.14 The absorbed power ratio vs. frequency for shield with 1μm thickness and various conductivities, which is placed in the middle SiO_2. In this graph conductivity is designated as s.

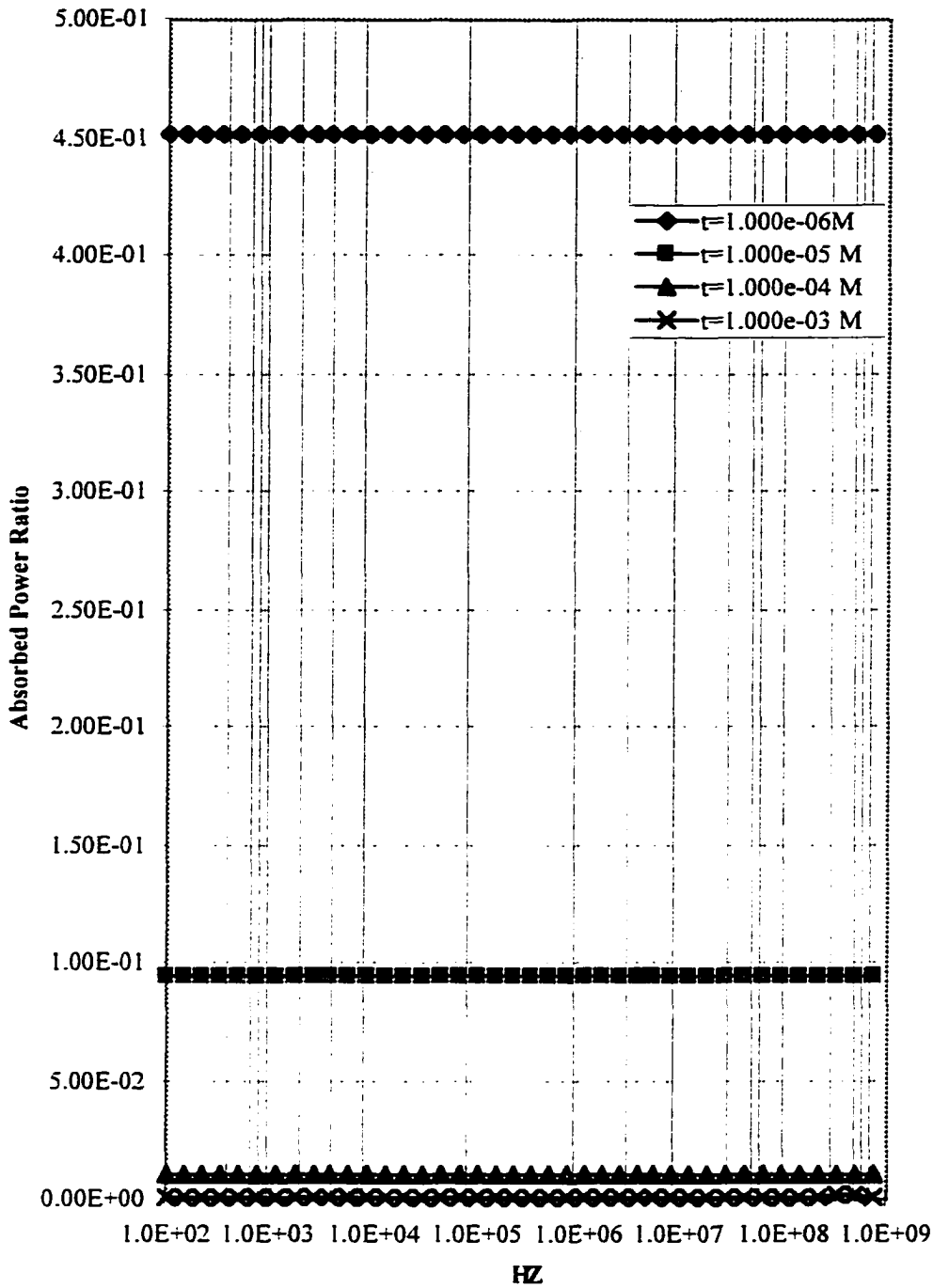


Fig. 2.15 The absorbed power ratio vs. frequency for shield with 2E+4 Ohm-M conductivity and various thicknesses, which is placed in the middle SiO_2.

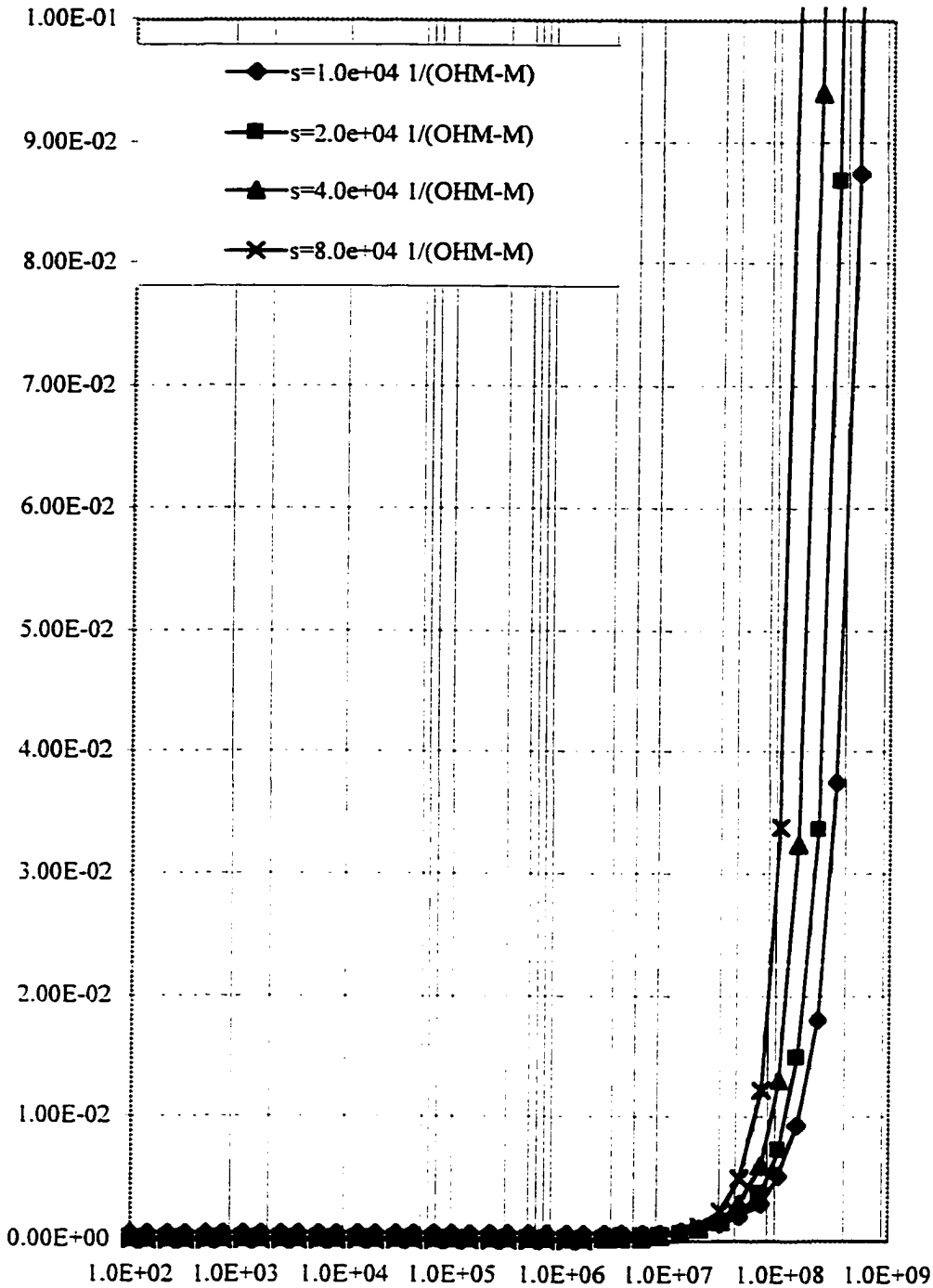


Fig. 2.16 The transmitted power ratio vs. frequency for a 2 mm thick shield with different values of conductivity. In this graph conductivity is designated as s.

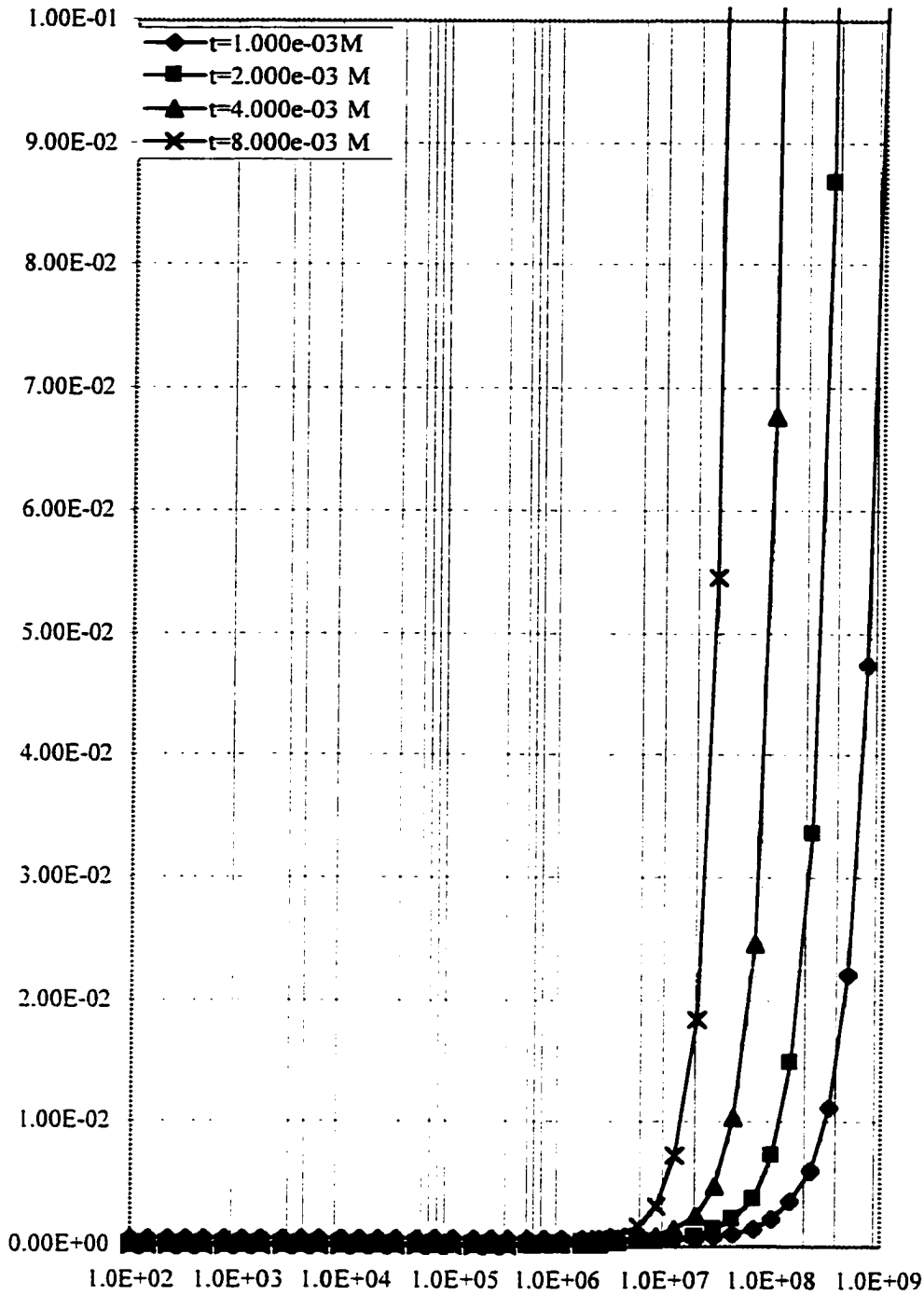


Fig. 2.17 The absorbed power ratio vs. frequency for shield with 2E+4 Ohm-M conductivity and various thicknesses, which is placed in the middle SiO_2.

2.2. Heat and Power Dissipation Considerations

Power dissipation and over-heating has always been a consideration factor in semiconductor technology. This fact is obvious in TTL, PMOS, ECL, and other technologies. Even for CMOS technology, where circuits are charged in a logical states and little leakage current is following through the devices, the power dispassion can limit the speed of the circuits built on a chip.

Obviously, the faster the switching speed is, the higher is the charge transfer will be. This results in more power dissipation. The power dissipation in CMOS technology can be calculated as:[16]

$$P_I = I_I \, V_{DD} \text{ (Static power dissipation)} \qquad \text{Eq. 2.53}$$

$$P = C_L \, V_{DD}^2 \, F \text{ (Switching Power dissipation)} \qquad \text{Eq. 2.54}$$

Where F is the frequency, C_L is load capacitance, I_I leakage current and V_{DD} is the supply voltage. It is an obvious fact that overall power dissipation of an IC should be kept below the maximum power dissipation limit. This maximum power dissipation limit is a function of thermal resistivity of the IC.[17]

Theoretical study shows thermal resistivity changing very little with an increase in the number of stacked layers. Fig. 2.18 shows the thermal resistivity as a function of the number of active layers.[17]

2.3. Device Isolation Consideration for 3DI Technology

Another very important issue related to 3DI technology is the issue of device isolation. Currently, there are several methods for device isolation available are utilized in various semiconductor technologies. However, not all these methods are compatible with 3DI technology. Here, a review of a few compatible methods are presented.

2.3.1. Device isolation by means of oxidization

One of the oldest methods utilized for device isolation is the oxidization method. In this simple yet very effective method an oxidized wall is created around the device or the devices, as shown in Fig. 2.19. The oxidized wall surrounding the device is connected to insulator under the active layer on one side and the isolator above the active layer on the other side. The major advantage of this method for 3DI technology is that the oxidized wall acts as a diffusion barrier. Of course, one of the disadvantages of this method is in the fact that the many oxidizing processes have high temperature requirements. Therefore, the correct oxidization process should be chosen. Moreover, the impurity redistribution between oxide and semiconductor, which takes place in their interface, should also be taken into account. Further more, the predicaments associated with GaAs oxide, in case of GaAs technology, prevents an effective use of this isolation technique.

2.3.2. Device Isolation by Means of Schottky Barrier

A new method, which is proposed by this paper, utilizes a Schottky barrier to isolate the devices on each layer. Fig. 2.20 demonstrates this method. In this method, a ring or rectangular shaped metal is placed around the device on the semiconductor's surface. The work function of the metal and the electron affinity of the semiconductor is chosen such that the Schottky barrier, resulting from this contact, extends all the way to the insulator that is located under the semiconductor. This means all the mobile charges, which are mainly responsible for current conduction are removed from this region. Therefore, this space is left with stationary charges. This phenomenon creates an energy barrier between the two regions, which should prevent from current movement between the two regions. One advantage of this technique is its low temperature requirement. Furthermore, this isolation method is more suitable for GaAs

technology. Of course, one of its potential disadvantages is its sensitivity to high temperatures. High temperatures may result in diffusion of metal inside the semiconductor.

Indeed, the popular method of back biasing of a PN junction is not appropriate for 3DI technology. This is due to the fact that the impurity redistribution between the P and N regions may damage the devices on the chip.

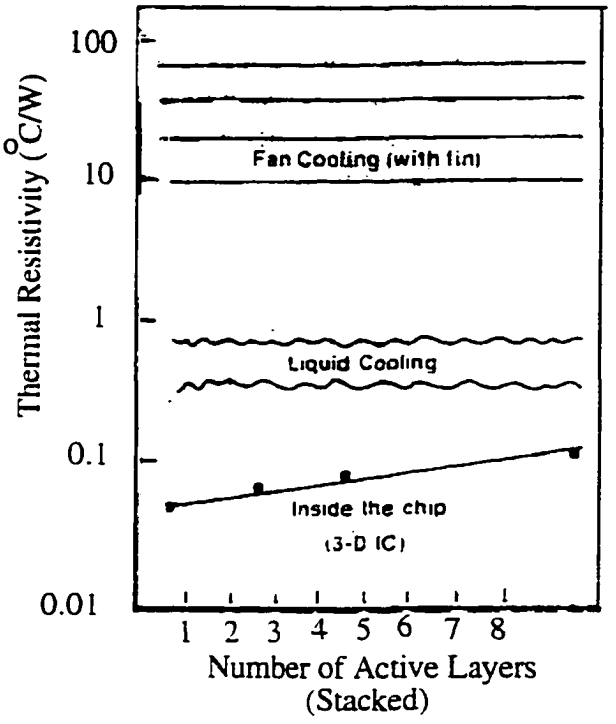


Fig. 2.18. Thermal resistivity vs. number of active layers constructed on a chip. It is assumed that the thickness of the active Silicon layers are 2μm and the passive SiO_2 layers are 1μm. [17]

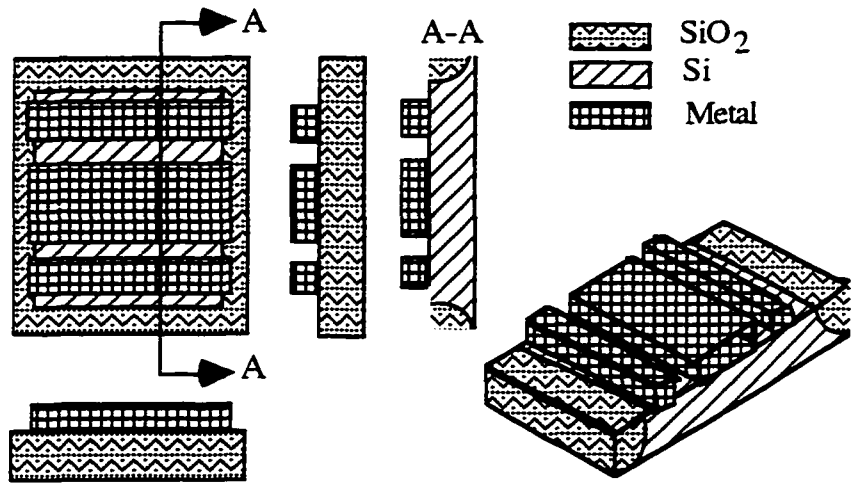


Fig. 2. 19. Device isolation using SiO_2 walls around the device.

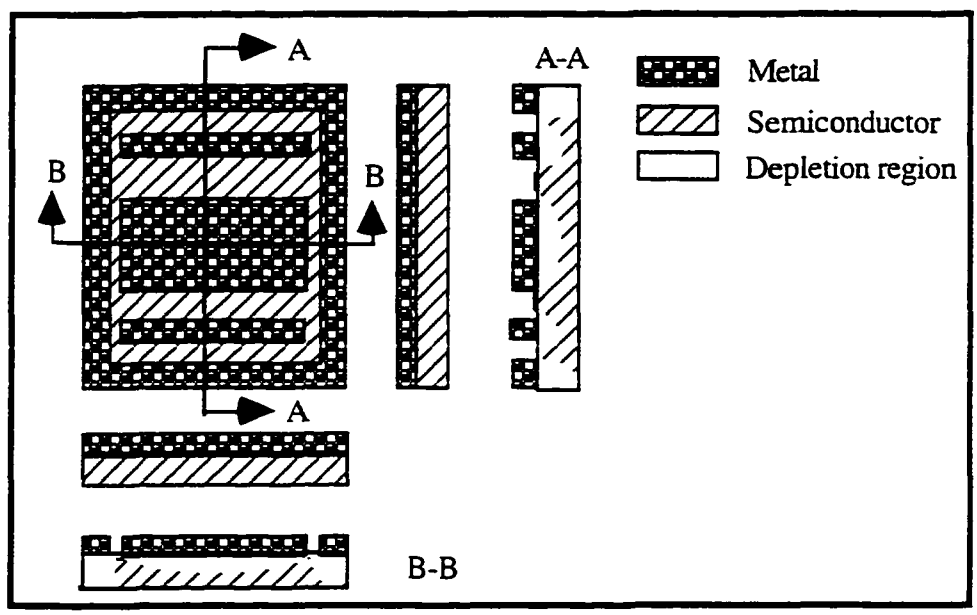


Fig. 2. 20. Device isolation using Schottky barrier technique

3. FABRICATION PROCESS FOR 3DI TECHNOLOGY

In previous chapters, the relevant technologies essential for development of 3DI technology has been reviewed. In this chapter, first a review of early attempts for fabrication of 3DI technology is presented. Then, a new fabrication process will be proposed. This new fabrication process, which will be presented at the end of this paper, will utilize the technologies reviewed in previous chapters.

3.1. Early Attempts in Developing 3DI Fabrication Technology

One of the earliest attempts made to stack several layers of circuits on top of each other was at the packaging level.[18] In this technique, first the wafers process independently and then these wafers are stacked mechanically at the packaging level. Fig. 3.1 and 3.2 demonstrate this technique. Usually, in-between the layers a masking layer is used, which is very similar to a PC-Board. This is done for two reasons. First, to make the connection in between the layers easier. Second, to make these connections more uniform from one IC to another. This is very important in cases where the shape of the connection changes the characteristics of the circuit, such as RF circuits. Furthermore, as it is shown in Fig. 3.2, "Bonding Pads" are utilized in between the layers to facilitate the electrical connection in-between the layers.[18]

The biggest advantage of this technique is its simplicity. On the other hand, the major disadvantage of this technique is its limitation of the number of connections that can be made between the layers. The biggest limiting factor for these types of connections is the size of connection pads: "Bumbs". The larger these pads are, the higher the reliability of the connections. In order to achieve reasonable reliability with these pads, they can not be made smaller than a given size. This "smallest size" depends on the particular technology.

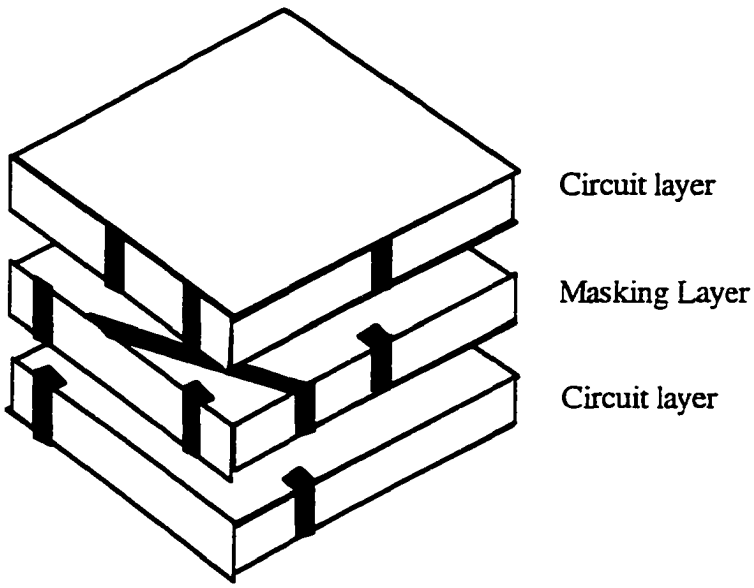


Fig. 3.1. Packaging level 3DI, utilizing interlayer musk.

In 1984, a paper was presented by M. Yasumoto, H. Hayama, and T. Enomoto of NEC's Microelectronics laboratories that suggested a new technology for stacking the layers on top of each other.[17] In this technique, two wafers are attached face to face, as shown in Fig. 3.3 and 3.4.

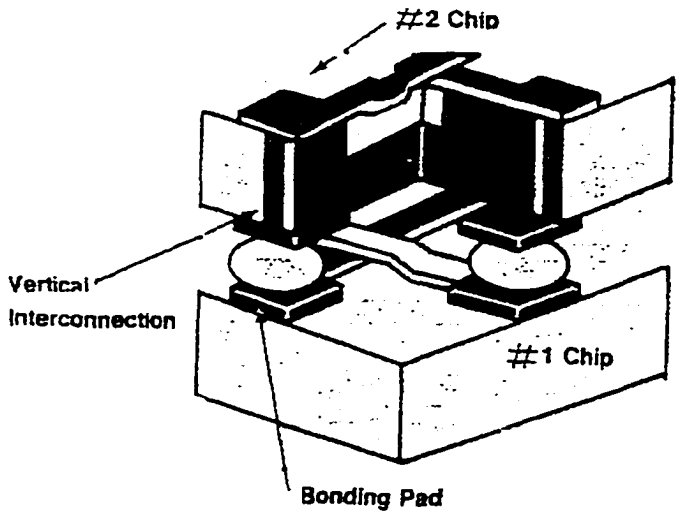


Fig. 3.2. Bonding pad used to connect two layers.[18]

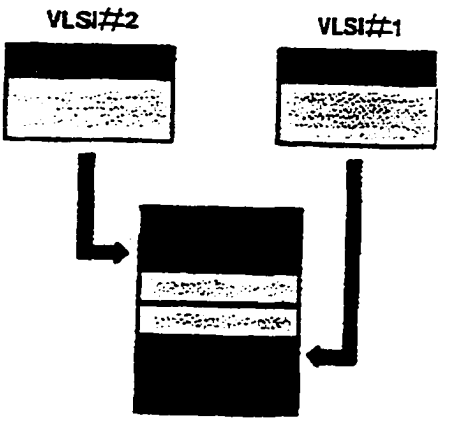


Fig. 3.3. Flip-chip 3DI technology. These layers will be connected using pressure.[18]

In this technique, first, each layer is fabricated independently using conventional fabrication technologies. Each layer ends up with Au Vertical Interconnections (VIs), which are formed in the last processing step of its fabrications procedure. These VIs had a cross section of 10 μm X 10μm and height of 2 to 3 μm, when this technology was originally introduced.[17] However, smaller dimensions can now be achieved using more recent technology.

The next step in this technology is to planarize the surfaces of these layers. The preferred planarization technology in this process is a spin-coating of polyimide on top each layer, as described in sections 1.2.3.1.1 and 1.2.3.1.3. This procedure follows by the alignment and thermal compression steps. In these steps the layers are aligned and placed face to face, using an "off axis system".[17] At the final stage of this technology, these layers are "thermally compressed". This final stage will connect and fuse the VIs of the two layers. The report indicates that about 52,000 VIs of 10 μm X 10μm size are perfectly connected in an 5 X 5 mm^2 surface area.[17]

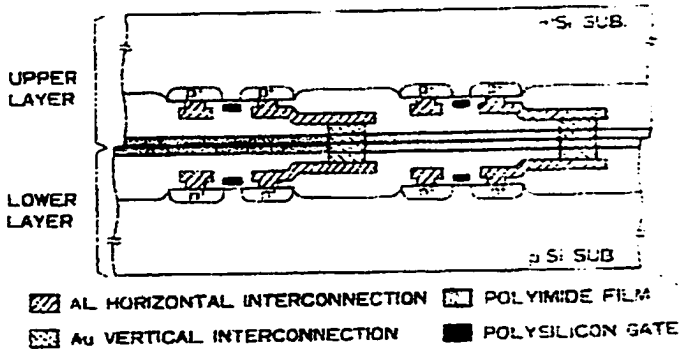


Fig. 3.4. A cross section of a Flip-Chip 3DI technology.[17]

While, this method dramatically increases the number of the connections made between the two layers, the process of stacking the layers is still very mechanical.

The first attempts to stack several devices on top of each other by means other than the mechanical was to stack passive elements. This was done using a technology similar to today's multilevel interconnection of VLSI circuits. This method, which is very popular today, proved to be very useful for memory chips. Capacitors in DRAM and resistors in SRAM can now be stacked on top of an active layer, leaving more room for active elements on the original wafer. As a result, chips with more memory are available today.

Later on, Stacked Transistor CMOS (ST-CMOS) technology provided the first non-mechanical means to stack the active layers as well. This technology is shown in Fig. 3.5.

ST-CMOS technology is really a NMOS technology that is converted to CMOS technology.[19] A n-channel MOS is fabricated using normal technologies. At the stage when the polysilicon gate of the device is being deposited, part of polysilicon of the gate is oxidized and some of this oxide is removed to achieve planarization. To create n^+ drain and source regions, a phosphorus predeposition is carried out after these areas are patterned.[19] The

second gate oxide is grown at approximately 1100°C. Note that this is a thinox and not the field oxide; therefore, a careful monitoring of this step is mandatory. At this point, a photolithography and masking step is necessary to etch a via hole for connection of the drains of the transistors (the top p-channel and bottom n-channel transistors). Now, it is the time to deposit the second polysilicon layer (poly II). This polysilicon layer is deposited under the same condition as the first one (the one that was used for the gate).

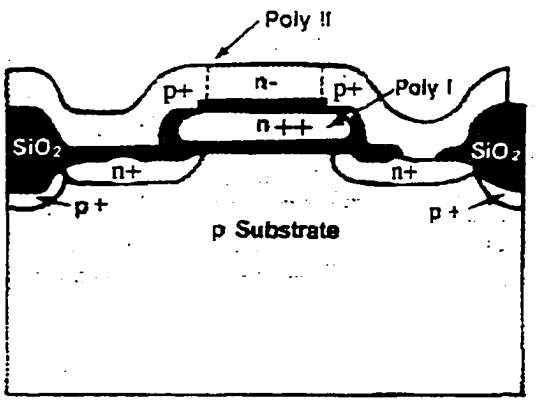


Fig. 3.5. A ST-CMOS inverter.[19]

Up to now, there are very few differences between this process and the NMOS process. From here, a few slightly different steps should be taken to complete the manufacturing process. First, adjustment should be made in the threshold voltage of the upper transistor. This is done by utilizing phosphorus implantation. Second, the source, the gate, and the drain areas are patterned such that they can be recrystallized using a laser recrystallization method. Finally, the source and the drain regions are heavily doped. This is usually done by an ion implant of boron ions in those regions. From this point, the process is

very similar to the regular NMOS process. That is, oxide capping, opening of the contact holes, aluminum deposition, and metal patterning, packaging, etc are all performed.

To visualize the extent of space that ST-CMOS technology saves in comparison to the regular CMOS process, Fig. 3.6 presents a simple inverter both in CMOS and ST-CMOS technology.

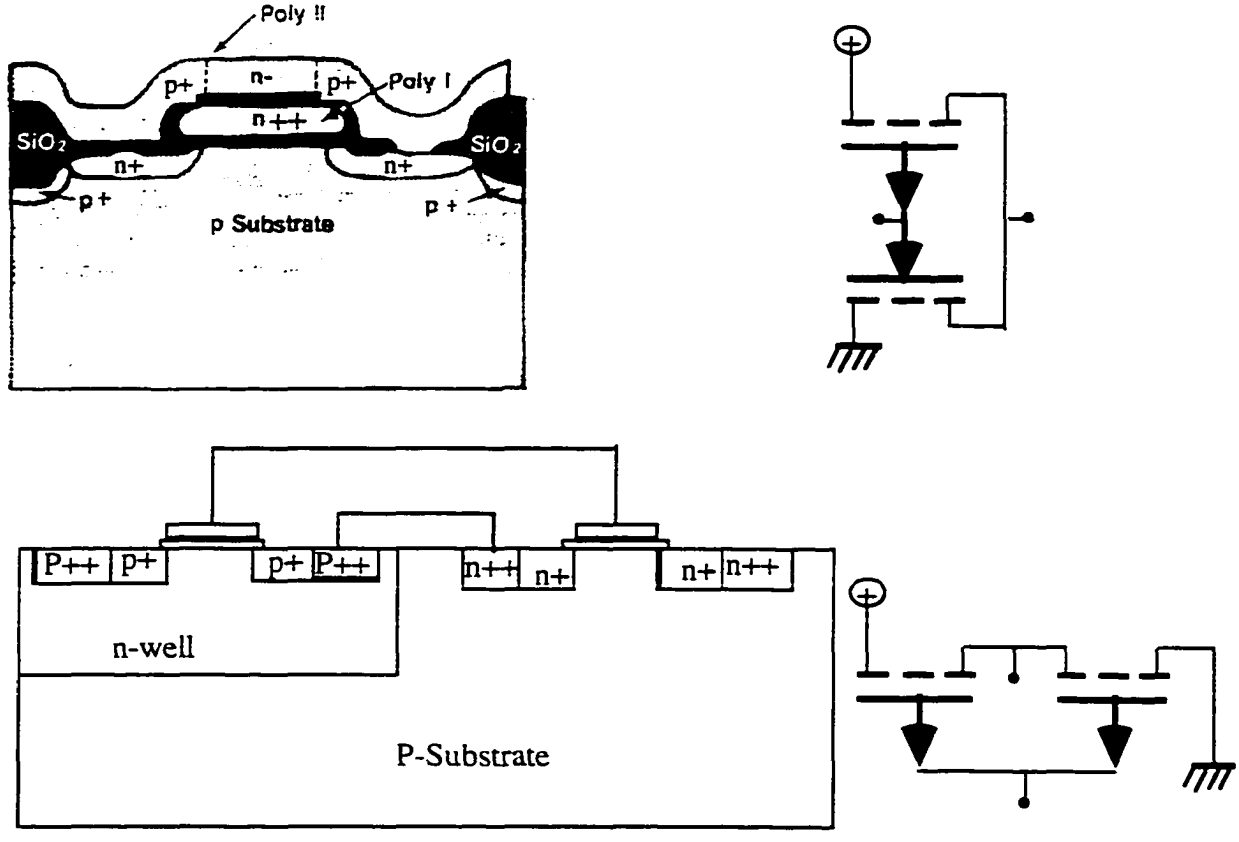


Fig. 3.6. An inverter both in CMOS technology and in ST-CMOS technology. The space saving on the original substrate is better than 2 to 1.

The advantages of this technology over regular CMOS technology are:[19]

1. Absence of a space consuming P or N well.

2. Stacking of the layers on top of each other.

3. Latch-up Immunity[1]

Of course, this technology has a few disadvantages of its own. The biggest disadvantage of this technology is the large source-gate and drain-gate capacitances in the top transistor.[19] This is due to the fact that major part of the source and the drain of the top transistor is fabricated on top of the gate, as seen in Fig. 3.5. These capacitances become more significant at higher frequencies. This technology has been reviewed extensively by Malhi et al[20] and Colinge et al[19].

Finally, the latest 3DI technology, which has been under development in recent years, is the stacking of several CMOS layers on top of each other. This technique, shown in Fig. 3.7, has many similarities to the technique that will be proposed by this paper; although, the proposed technology in this paper uses different type of device and includes major additions and revisions to this simple stacking technique. These changes, presented in the next section, are designed to eliminate the problems associated with this simple stacking technique. Moreover, a great deal of effort has been made to find the most suitable processing procedure compatible with the over all requirements of this technology, for each processing step.

---

[1] Latch up is the unwanted creation of parasitic transistors and diodes from the interactions of the p-wells or the n-wells with the transistor structures used for fabricating the circuit. These parasitic diodes and transitors can create short circuits in-between the Vdd and Vss.[21]

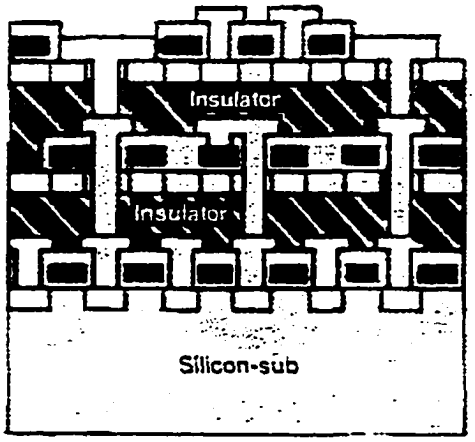


Fig. 3.7. Simple stacking of the CMOS layers on top of each other.[17]

Due to the fact that simple stacking of the CMOS layers can be, for most part, considered as a subset of the technology that will be proposed by this paper, no further discussion of the simple stacking of CMOS layers will be presented here. The interested reader is encouraged to refer to references given at the end of this paper. Moreover, no standard processing procedure has been developed for simple stacking of CMOS layers at the this time. Here, it should be noted that the major differences between the technology proposed by this paper and the simple stacking of CMOS layers technique are the active devices utilized to fabricate each layer, interlayer shield, and the individual processing procedures for each step.

3.2. Proposed Advanced Stacked Layer Technology and Its Fabrication Process

So far, an overview of all the relevant techniques that might be useful for 3DI technology and previous attempts to develop a 3DI technology has been presented. It is prudent in developing a new technology that we first critique these previous attempts. The

knowledge gained from this critique can help to better design a new technology. Therefore, the next subsection shall be devoted to evaluating these previous attempts in 3DI. Finally, procedural instructions for production of 3DI chips will follow that subsection.

3.2.1. Lessons From the Previous Attempts

One of the biggest lessons from the past experiences in the development of 3DI technology has been this: have as little impurities on each layer as possible. Most previous attempts for creation of 3DI technology were proscribed by the reality that multi-impurity devices have been used in them. Therefore, here an attempt will be made to develop this technology based on single impurity device SOI-SBSD-MESFET , which is described in Sec. 2.2.2. This device, which has been specifically developed in this paper for use in 3DI technology, has only one type of impurity form. Furthermore, to even better condition this technology for several re-heating steps required for fabrication of many layers, only one type of impurity will be used on each layer.

Another important lesson from the previous attempts in development of 3DI technologies is the presence of cross-talk. To solve this problem a grounded shield layer will be placed in-between the circuit layers. This layer can be made from metallic materials, which can be implanted in-between a thick layer of insulator, or a heavily doped poly-silicon layer. Furthermore, the technology proposed by this paper recommends shielding the vias, as shown in Fig. 3.8, if they are placed too close to each other. This shield should prevent the cross talk in-between the layers. A note is in order here: not all the vias should be shielded. Only those vias that are placed very close to each other, which might create cross talk on each other, should be shielded.

The need for planarization has created another important lesson. This fact becomes very obvious if one considers the accumulated effects of placing several layers on top each

other. Therefore, various planarization techniques have been reviewed in section 1.2.3. Here, a combination of these techniques should be employed, in order to achieve the best result.

Furthermore, the fabrication procedures, utilized in this technology, should have low temperature requirements. This is due to the fact that high temperatures damage the circuits already built in the previous layers. Therefore, depositing key materials at low temperatures is the golden key to success in this technology.

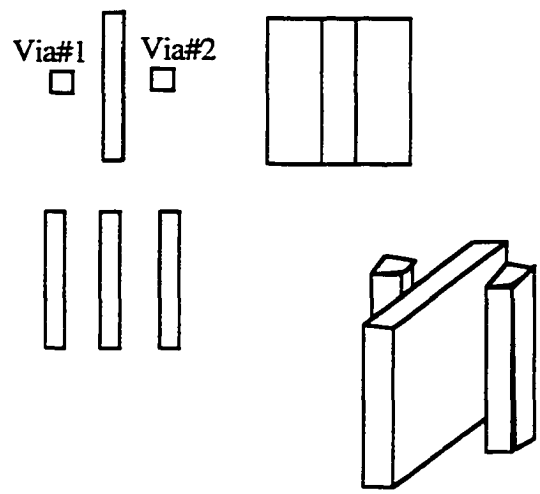


Fig. 3.8. A shield layer in between vias to prevent cross talk between them.

The last, but not least, is the characteristics of the deposited semiconductors. Since the semiconductor is deposited at low temperatures in order to prevent damaging the previous layers; its characteristics are not good enough for fabrication of active devices. Therefore, somehow these characteristics should be improved. Appendix A.2.4. describes various techniques for improvement of the characteristics of the deposited semiconductor. Here, in this

proposed fabrication technology laser recrystallization, one of the previously described techniques, will be used extensively for improvement of the deposited layers.

These enumerated along with many other unenumerated facts were taken in to full consideration in design of the proposed fabrication technology, which will be presented next.

3.2.2. A Proposed Fabrication Process for 3DI Technology

In order to describe this repetitive process, one should start describing the process from one stage of a layer to the same stage of the next layer. To construct the following layers the same procedures will be repeated several times. This process may start at recrystallized semiconductor on insulator and proceed onward. Fig. 3.9 presents the wafer at the beginning of the first stage.

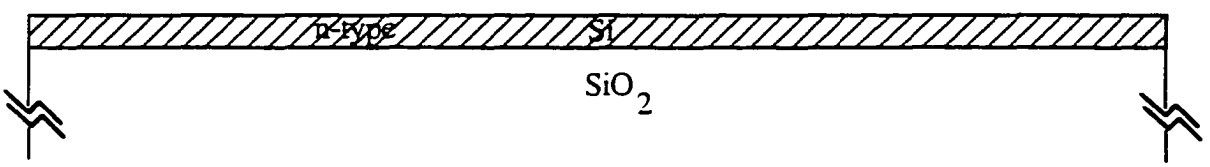


Fig. 3.9. The wafer at the beginning of the process.

To produce the first SOI layer, a number of different methods can be employed. Among these techniques are seeding along with the laser recrystallization technique (both of which will be employed for creation of upper SOI layers) and ion implant of Oxygen ions underneath the silicon. Alternatively, the process might start from a SOI substrate. SOI substrates have many advantages over regular substrates including larger dimensions, which will be beneficial for mass production.

In the first stage of the production the gate metal, or alternatively the gate metal-silicide, is deposited. This may be done using the processes outlined in Apendix A.2.2.3 through A.2.2.4. The thickness of the SOI layer and the work function of the metal are related, as described in sec. 1.2.2.2. The metal should be chosen based on its work function, so that the metal makes a rectifying contact with the semiconductor. Furthermore, the thickness of the SOI layer should be such that the depletion region underneath the gate extends all the way to the insulator layer beneath.

This step follows a lithography and etch process to remove the metal from the unwanted area of the semiconductor. Fig. 3.10 shows the wafer after this stage.

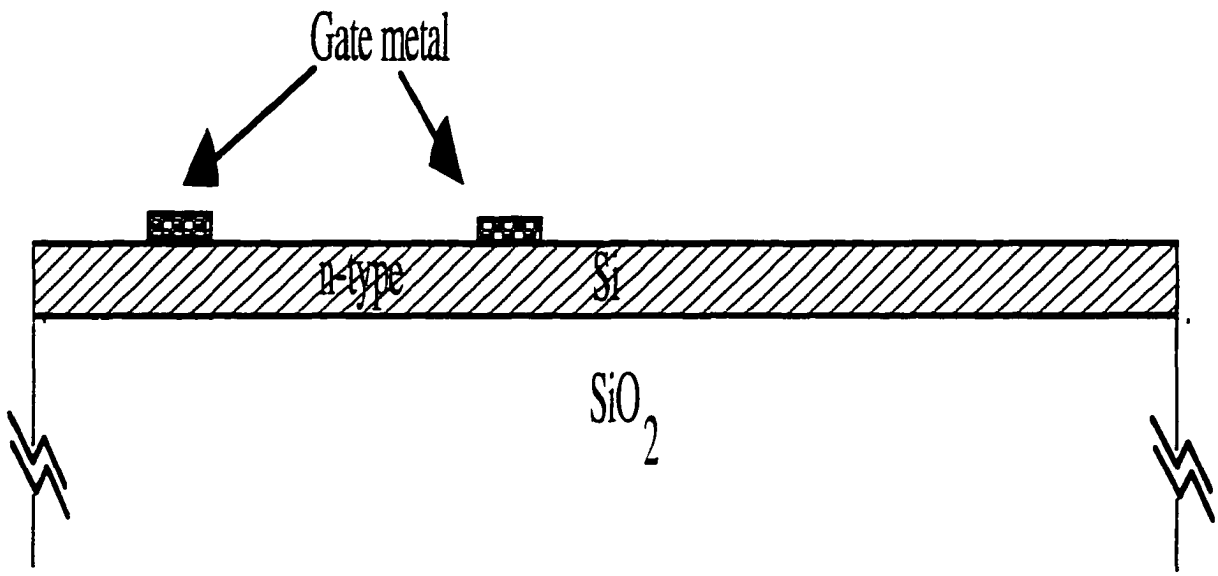


Fig. 3.10. Substrate after the gate metal or metal-silicide is deposited.

Next, a thin layer of oxide is deposited on top of the wafer. The quality of the oxide is not as important as the thinox is in a MOSFET; therefore, this layer can be deposited using the procedure described in section 1.2.2.2.1. The thickness of this layer is of little importance, since the only function this layer plays is to insulate two metals layers from each other. Therefore, as long as this layer is thicker than a couple of tenths of micron, it will function fine. Fig. 3.11 shows the substrate at the end of this stage.

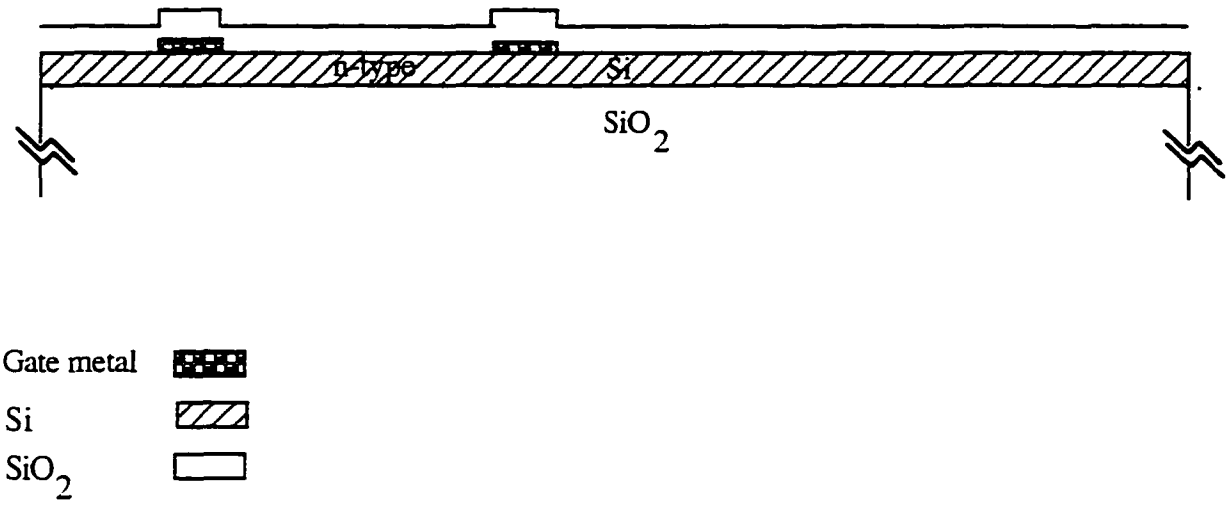


Fig. 3.11. Substrate after the oxide layer is deposited on top of it.

Following this stage, it is the time for an optional stage for oxide insulation of the devices. This step is totally optional, since device isolation can be achieved using Schottkey barrier insulation technique as mentioned in section 3.3.2. In the case of the Schottkey barrier insulation technique, a metal ring or polygon is placed around the device, so that it totally

surrounds the device. This can be done at the same time as the gate metal is deposited. This reduces the number of processing steps and increases the yield.

Nonetheless, if the decision is made decided to isolate the devices using an oxide technique; it can be done at this stage by a combination of wet oxide at 600°C, and multi-oxide implant.[22-24] That is, the first substrate is multi-implanted with oxygen;[22-24] then the substrate undergoes the wet oxidation in another chamber at 600°C for short period of the time. The implanted oxygen makes the implantation time shorter. Without the multi-implant high temperatures and long exposure time is required to fully oxidize the area in-between the devices. Furthermore, ion implant damages the semiconductor crystal structure in-between the devices and as a result reduce the conductivity of this area even more. Fig. 3.12 shows the substrate after this stage. Of course, lithography and etch process precedes this step to lift the oxide from the top of the areas that need to be oxidized. As mentioned before, this step is optional and might be eliminated altogether.

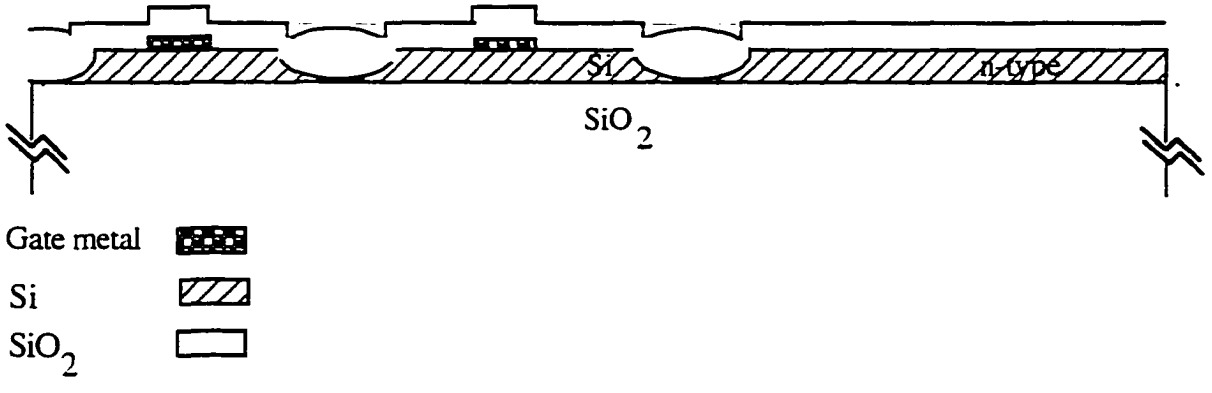


Fig. 3.12. Devices are isolated using oxide walls around them.

At this stage, a lithography and etch process follows to remove the oxide layer from the top of the source and drain regions. Moreover, the oxide is removed from the top of the gate metal, or the metal silicide, where there should be a contact between the gate metal and the source and the drain metal. The substrate after this stage is shown in Fig. 3.13.

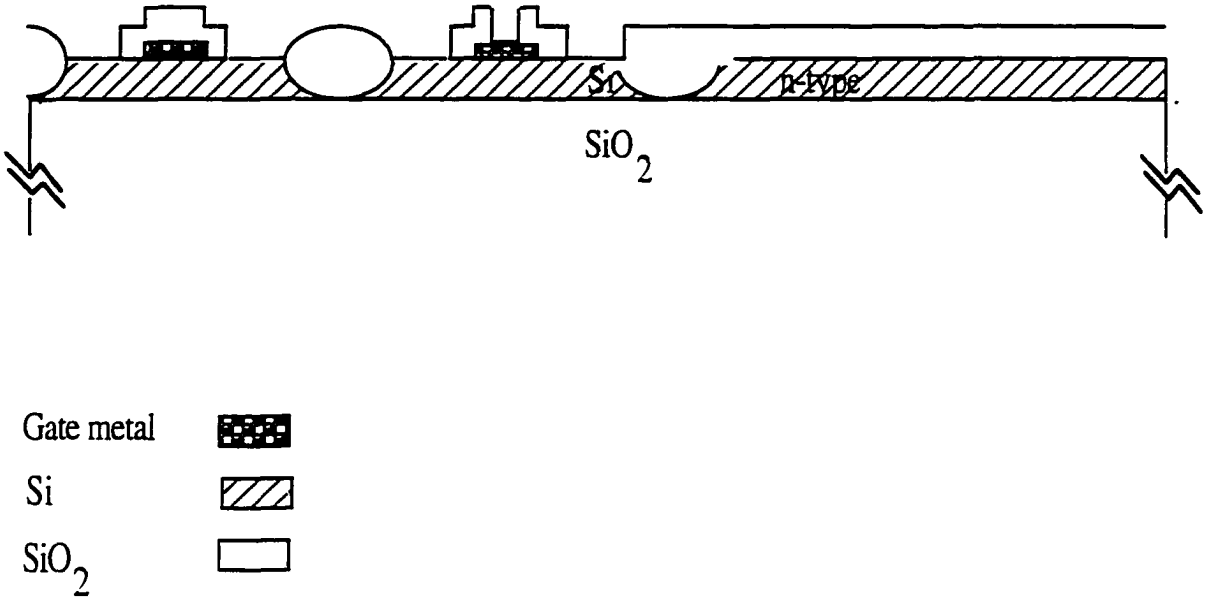


Fig. 3.13. Substrate after the oxide over source and drain is etched away.

Next, its time to deposit the metal, or the metal-silicide, of the source and drain. This metal is different from the gate metal, since its work function should be chosen to make an ohmic contact with the semiconductor, as it is described in section 2.2.2.2. The fabrication process for metalization itself has been described in Appendix A.2.2.3. through A.2.2.4. The substrate after this stage is shown in Fig. 3.14.

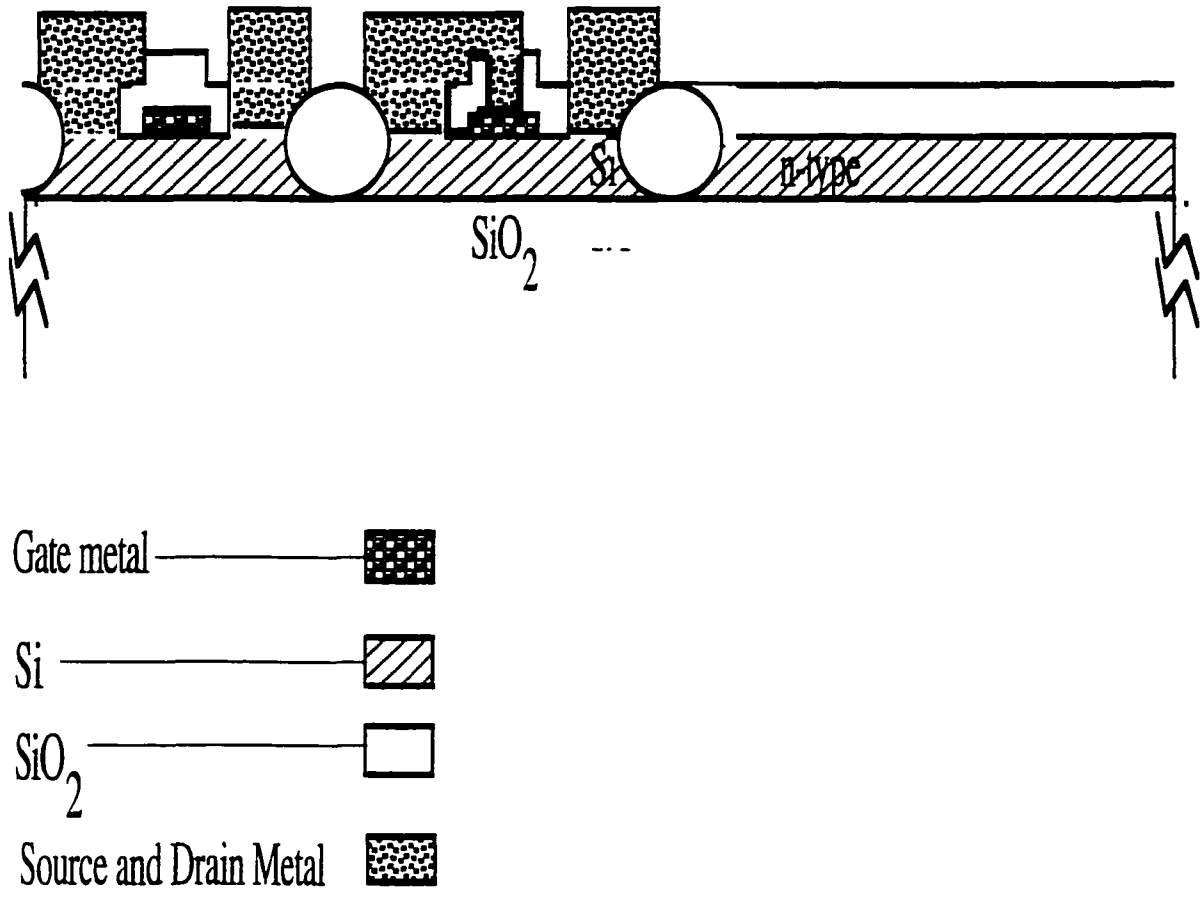


Fig. 3.14. Cross section of the substrate after source and drain is metalized.

At this point a planarization process is in order. Various planarization techniques have been reviewed in sec 1.2.3. It has been decided that Borophosphate Glass (BPSG), described in section 1.2.3.4, should be deposited by the spin on layer technique, which is presented in section 1.2.3.1. Following this step, sacrificial etch back technique should be employed to further planarize the substrate, as described in section 1.2.3.4. The substrate after this stage is shown in Fig. 3.15.

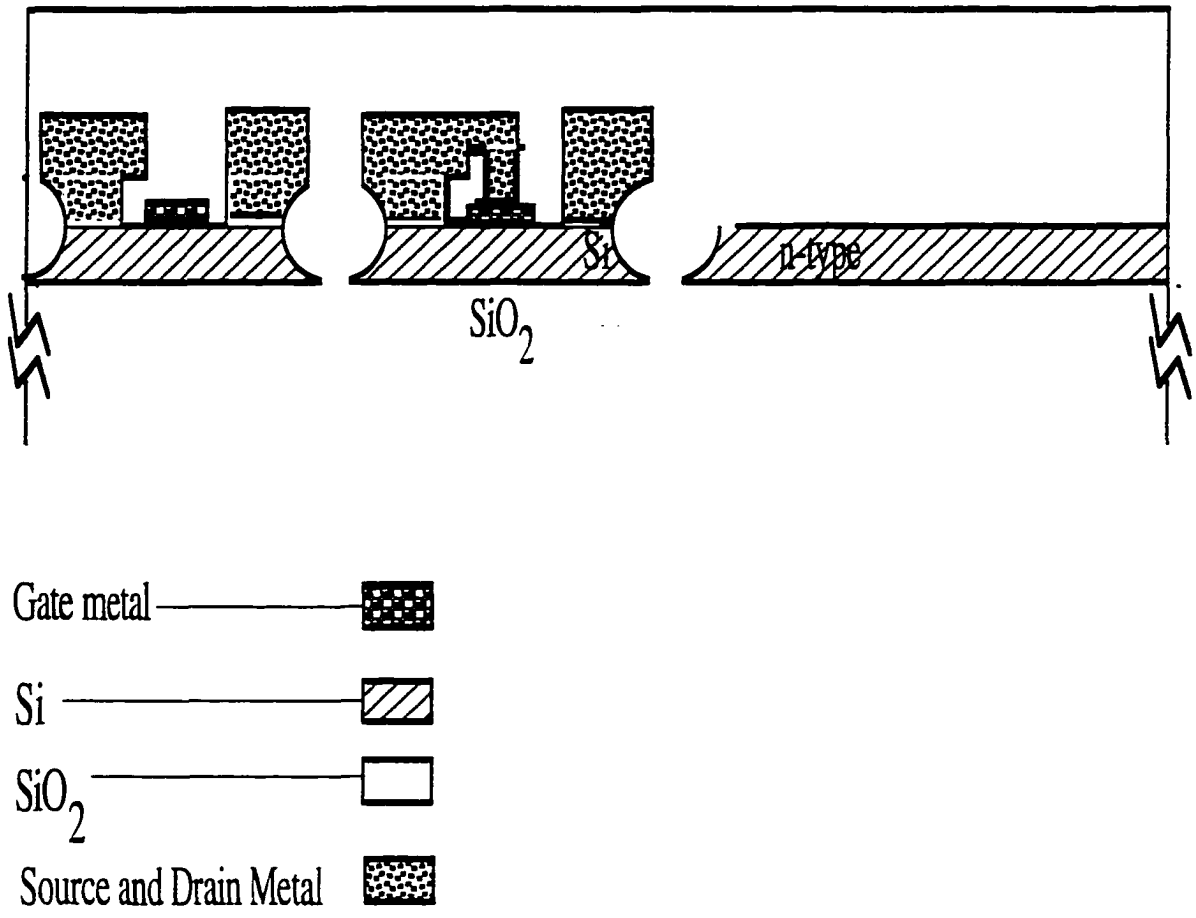


Fig. 3.15. A cross section of the substrate after planarization stage.

Now, it is the time for providing the connection in-between the layers. Therefore, the inter-layer vias are to be placed in this stage. This can be done using a dry etch to create the necessary holes on top of this layer, followed by metalization and patterning. A thin layer of oxide is placed uniformly on top of the substrate, using techniques outlined in section 1.2.2.2.1. The substrate after this stage is shown in Fig. 3.16.

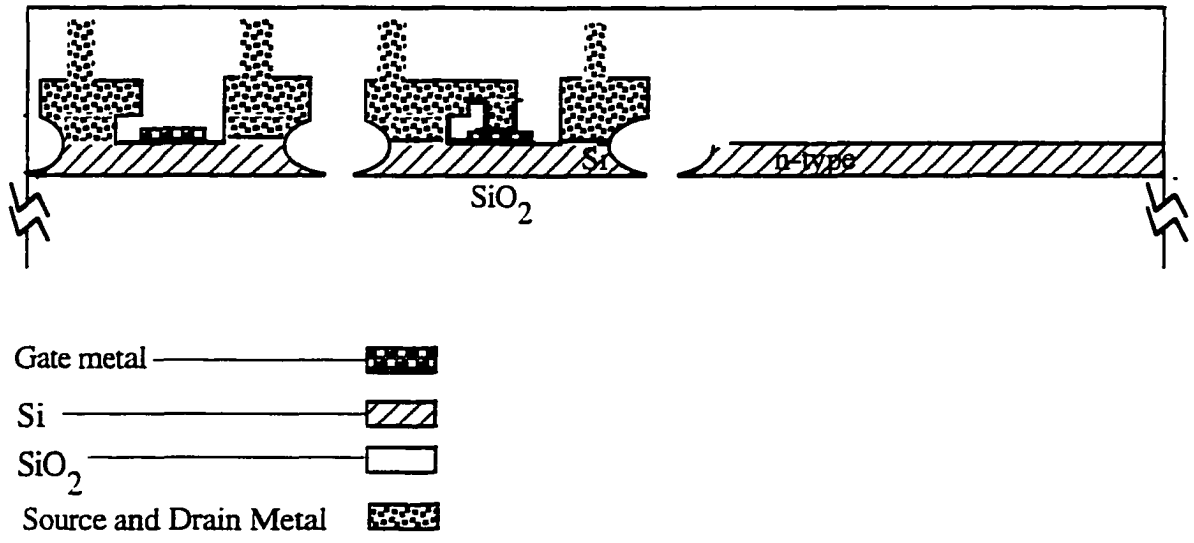


Fig. 3.16. A cross section of the substrate after vias and thin oxide is placed.

The seeding windows, described in Appendix A.2.4.1, should now be opened. This is done using the etch process. This stage follows by the deposition of the next layer. The semiconductor layer can be deposited, using a chemical vapor deposition described in Appendix A.2.2.2. Note that the deposited layer is a p-type polysilicon layer, not n-type. Following this step, the surface of the substrate is etched to achieve some additional planarization.

As it has been mentioned earlier, the characteristics of this layer should be improved in order to achieve devices with good characteristics. To improve the characteristics of this layer and to create large crystals suitable for device manufacturing, the laser recrystallization method should be utilized, which is reviewed in the Appendix A.2.4.3. The cross-section of the substrate after this stage is shown in Fig. 3.17.

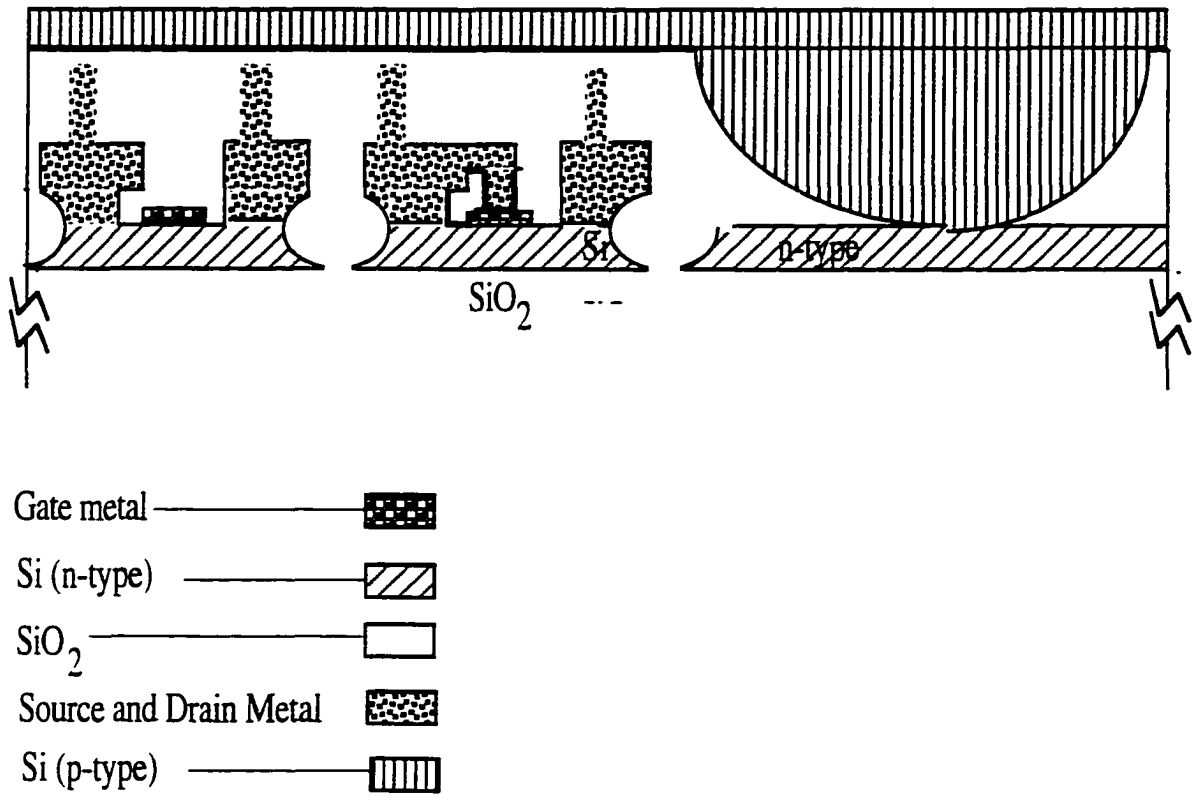


Fig. 3.17. A cross section of the semiconductor after the second layer is deposited.

Note that the thickness of this layer and work function of the gate metal is inter-related, as it is described in section 2.2.2.2. The metal should be chosen based on its work function; alternatively, the thickness of the layer should be adjusted according to the work function of the metal. Similar to the n-layer underneath this layer, the thickness of this layer should be such that the depletion region underneath the gate extends all the way to the insulator layer beneath.

Now, it is time to provide connection between this layer and the layers beneath it. To do this, first the location of these vias are oxidized. In order to keep the oxidation time and

temperature to a reasonable value, these locations are first multi-implanted with oxygen. Then, a short period of wet oxidation at 600°C follows. Finally, these locations are etched using dry etch process. After the via holes are created a metalization and patterning follows to complete this process. The oxidation around these vias is necessary to make sure there is no contact between them and the semiconductor. The oxide around these vias should be thick enough to prevent any interaction between the metal and the semiconductor. The substrate after this stage is shown in Fig. 3.18.

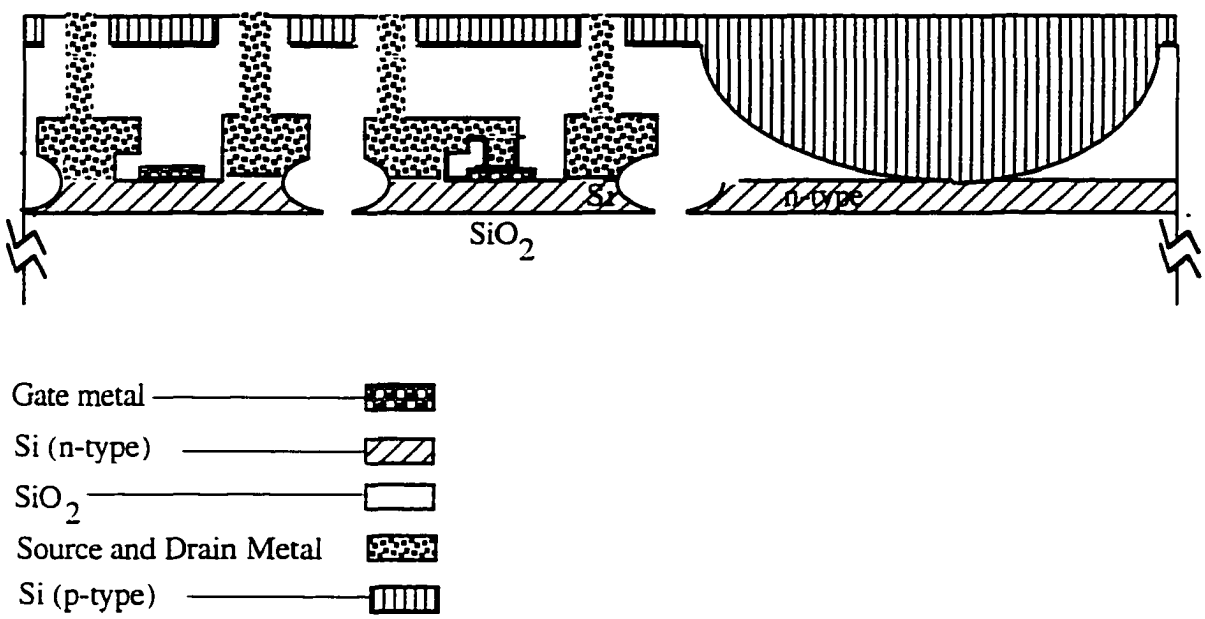


Fig. 3.18. A cross section of the substrate after vias are connected to the lower layer.

To complete this layer, steps similar to those that were carried out to complete the previous layer should be taken. After this layer is completed, another layer of heavily doped n-type polysilicon is deposited. The heavy doping is necessary in order to insure the low resistivity on this layer. As discussed in section 3.1.1.1, the resistivity of this layer should less than 0.01 Ω-cm. This layer need not to be recrystallized, since its only function is to be used as a shield layer. However, if the resistivity of 0.01 Ω-cm or less could not be achieved in a poly crystalline silicon, then every effort has to be made to insure the low resistivity in this layer. This includes recrystallization and addition of other impurity materials such as silver and metal implant in middle of this layer. Moreover, the shield layer should be grounded to eliminate the cross-talk between the layers. Fig. 3.19 presents a cross-section of a complete circuit layer, which consists of three semiconductor layers (a n-type, a p-type, and heavily doped n-type used for shielding).

This concludes the building of one period in this periodical layer structure. Subsequent layers can be built by repeating this process. This way, several layers of active devices may be stacked on top of each other. Fig. 3.19 presents several layers of semiconductor that are stacked on top of each other in this fashion.

Here, a final note is in order. As it can be seen from figures 3.18 and 3.19 the gate metal for a n-type semiconductor and the gate metal for p-type semiconductor are not drawn the same. This is done to demonstrate that these two metals need not to be the same. Of course, in practice one might chose the same metal for both p-type and n-type semiconductor gates. Such a choice makes it necessary to have different thicknesses of p-type and n-type layers, as described in section 2.2.2. Furthermore, the metal used for source and drain might not be the same in both p-type and n-type semiconductor. This is because a metal may make an ohmic contact with n-type of semiconductor and rectifying contact with p-type, thus making it necessary to use different metals.

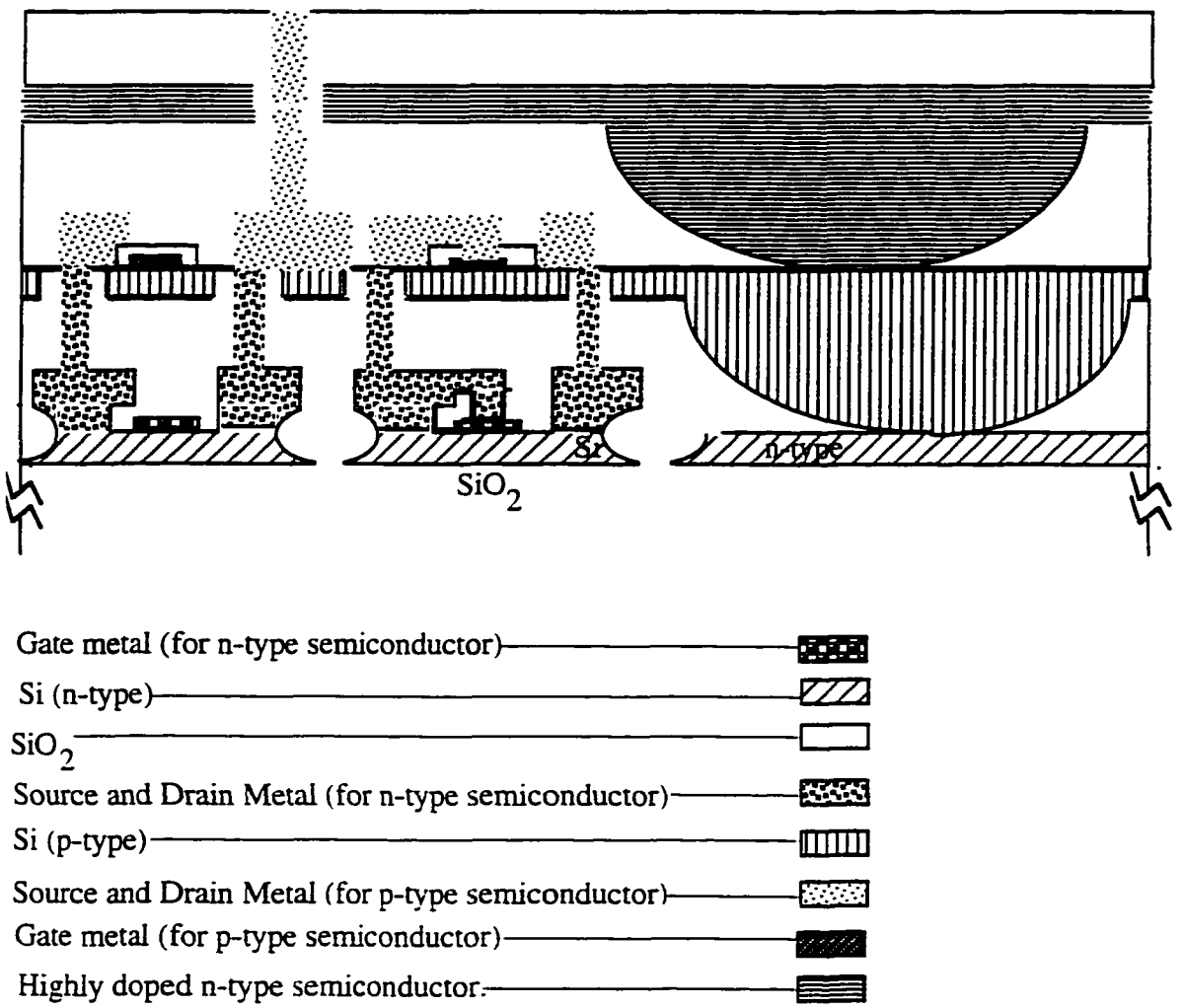
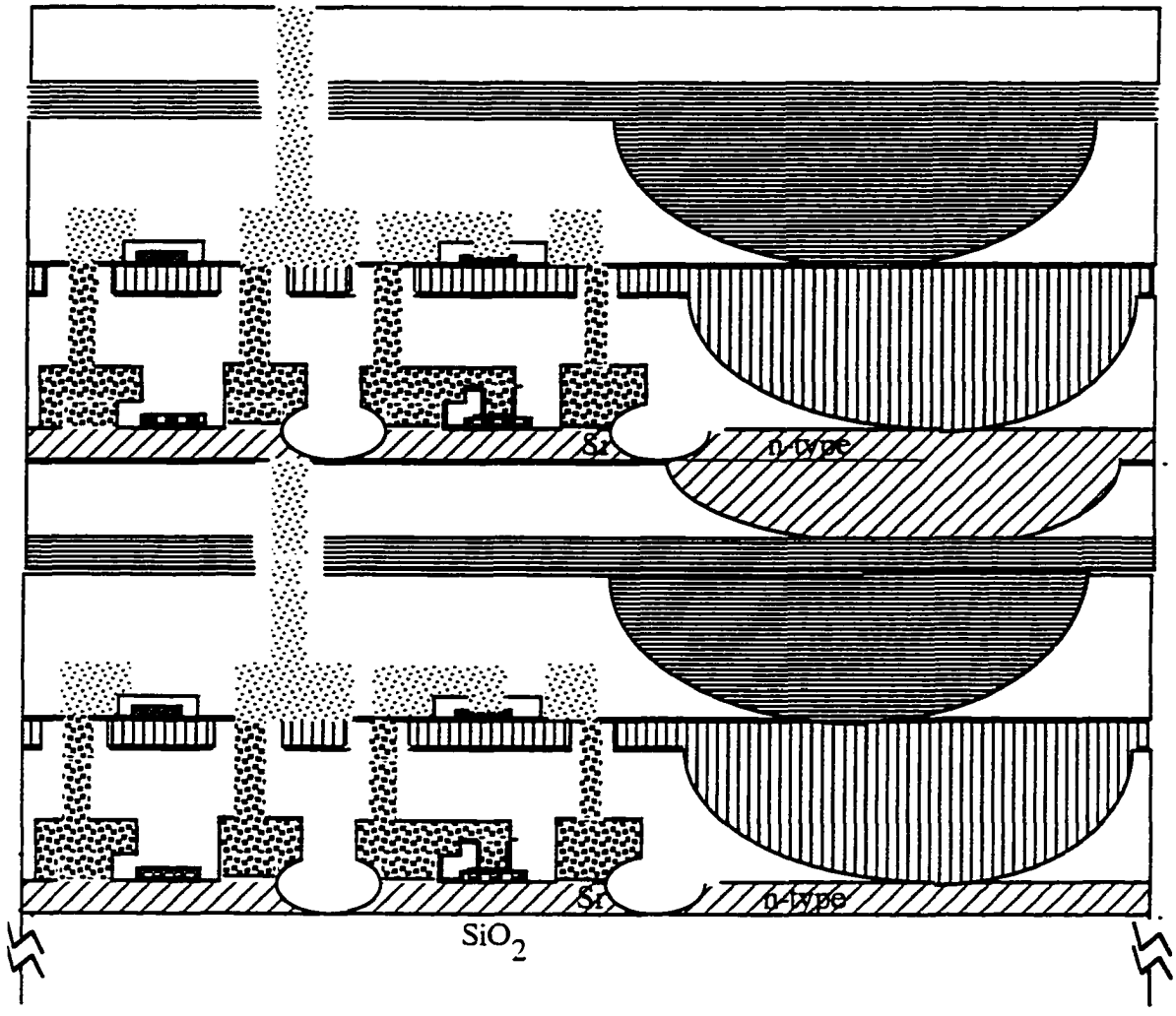


Fig. 3.19. Cross section of a complete circuit layer, which consists of a n-type layer, a p-type layer, and a heavily doped n-layer used as shield.



Gate metal (for n-type semiconductor)
Si (n-type)
SiO_2
Source and Drain Metal (for n-type semiconductor)
Si (p-type)
Source and Drain Metal (for p-type semiconductor)
Gate metal (for p-type semiconductor)
Highly doped n-type semiconductor

Fig. 3.20. Cross section of two stacked circuit layers (6 semiconductor layers).

4. ANALOG EXTENSION OF 3DI

Even though with the recent improvement in the science of Digital Signal Processing (DSP) and Digital Control, there seems to be no need for any analog circuits; many analog circuits still offer a substantial advantage over their digital counterparts in many areas. In fact, certain analog circuits can not be made using digital techniques with current technologies. Low noise pre-amplifier for electromagnetic waves is a good example of such a circuit. Moreover, a number of analog circuits, such as Analog Filters, require much less components and are easier to implement than their digital counter parts. In this section we would like to briefly review the specific requirements of this type of circuits and the way this type of circuit maybe implemented in a 3DI technology.

One of the differences between a digital circuit and an analog circuit is in the fact that an analog circuit uses considerable number of passive elements. Most passive elements are bulky. For example, a resistor might take as much as 40 times the size of a transistor in an integrated circuit. Moreover, due to small size of the chip, passive capacitors with values greater than a tens of pF and passive inductors with values more than a few nH are very difficult to attain. Therefore, in cases where higher values are required an active capacitor or inductor might be considered. First, let us review these important elements in more detail.

4.1. Inductors

Although, most chip designers try to avoid using inductors; there are times that inductors are unavoidable. The reasons for avoiding the use of inductors in the chips are:

- They take too much valuable real-estate.
- Only very low values of passive inductors are achievable on the chip.
- The tuning of such inductors is very difficult.

Nevertheless, these inductors are being used in microwave and high frequency circuits. The most common architecture of these inductors are presented in Fig. 4.1.[25]

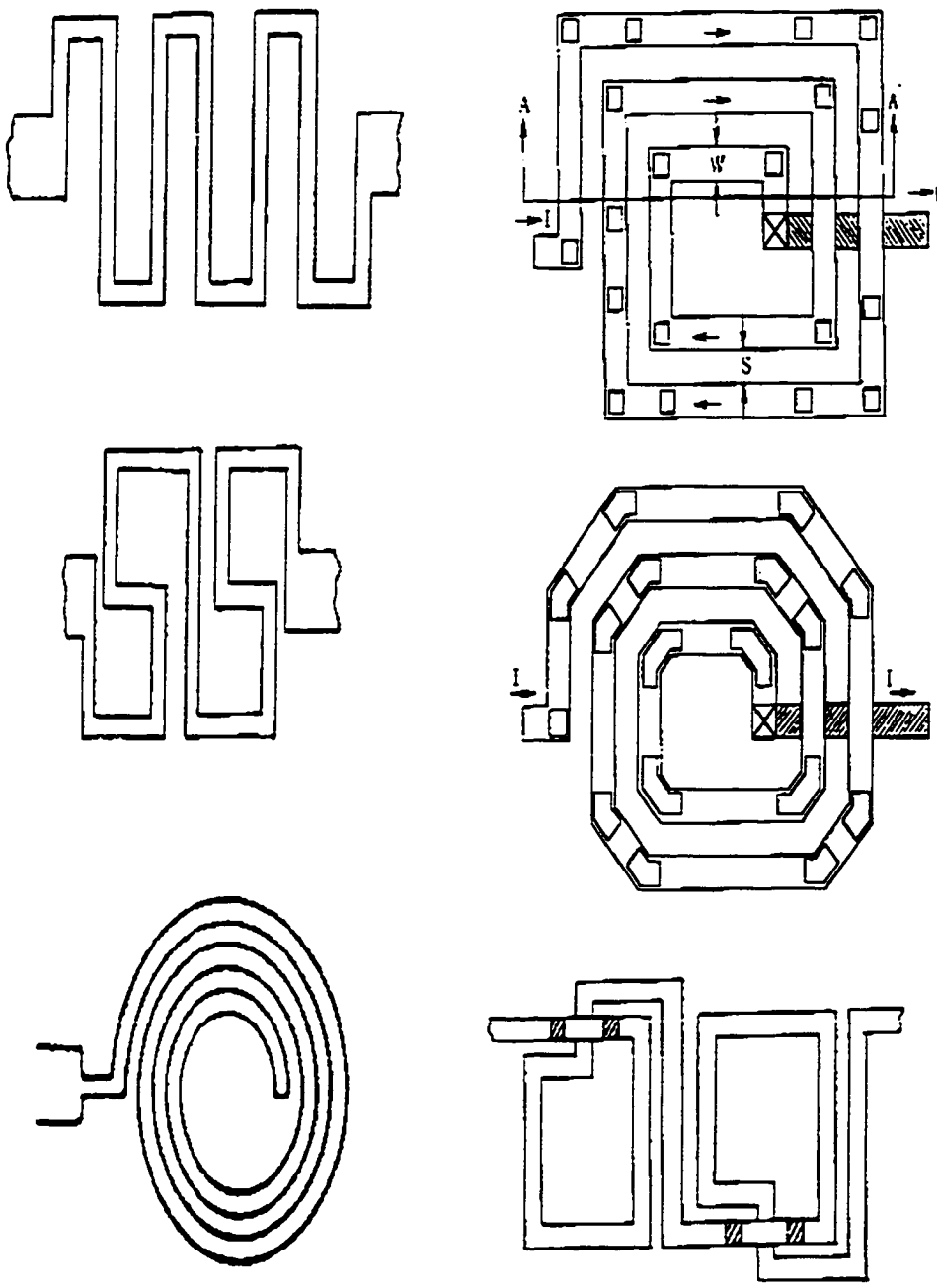


Fig. 4.1 Various forms of spiral passive inductor used in chips[25].

Another related issue is calculating the value of such inductor. This usually is done by computer simulation of such inductors. Even though, it has been reported that computer simulation for spiral inductor structures had resulted in a comparable value to the actual inductor's value; the circuit designers usually pick these inductors from a library of pre-proven designs for specific inductance value. It is important in simulation of these inductors that one pays special attention to image charges, which create an image inductors in the ground planes. Moreover, due to the parasitic capacitor effects in this types of inductors, the value of inductor may change as a function of the frequency. The result one of such simulation is shown in Fig. 4.2.[25] A listing for the simulation of the rectangular spiral inductor using Libra (a popular simulation program for microwave circuits) is given in Fig. 4.3.[26]

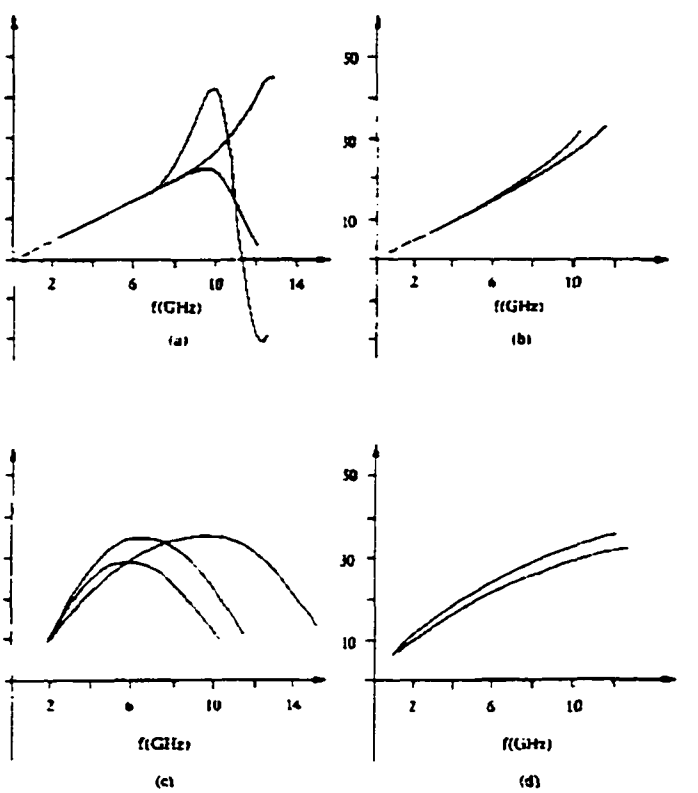


Fig. 4.2. (a) Spiral inductor reactance, (b) Single-Loop reactance, (c) Spiral inductor Q-factor, and (d) Single-loop Q-factor versus frequency.[25]

Rectangular Spiral Inductor Simulation

```
dim
        freq    hz
        res     h
        ind     nh
        cap     pf
        lng     mil
ckt
        mstub er=11.8 h=20 t=0.02 rho=1 rgh=0
        tand    tand=0.004
        mrid    1 0 n=3  l1=12  l2=12 w=0.4 s=0.4  w1=0.5  w2=0.5
       defIp  1 rect
freq
        sweep 0.1 3.0 0.1
out
        rect s11
        rect z11
! End of file
```

Fig. 4.3. Listing for simulation of a Rectangular Spiral Inductor using Libra (a popular simulation program for microwave circuits).[26]

Another way to achieve the characteristics of an inductor is by utilizing the characteristics of a transmission line. As shown in Fig. 4.4, a high impedance line can be utilized as an inductor or a capacitor. Utilizing this technique, whenever possible (i.e. high frequencies f >>1GHz), provide us with a wide range of inductor values.

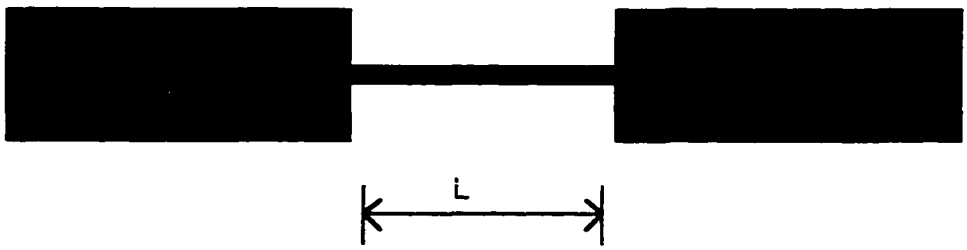


Fig. 4.4. Transmission line is utilized to realize inductive characteristics.

Finally the third way of creating an inductor is to design an active inductor. Many different forms of active inductors using various active elements have been proposed and studied;[26-29] However, the active inductors proposed by Hara et. al[28-29] are most suited for 3DI technology. These inductors are shown in Fig. 4.5.[28-29]

There are several advantages in utilizing active inductors for higher values of inductance. One of the most important advantage of an active inductor is its lower value of stray capacitance. This enables an active inductor to function at much wider range of operating frequencies than normal spiral inductors can. Moreover, in order to achieve high value of inductance (using passive inductors), several spiral inductors and transmission lines should be combined. This not only complicates the task of designing such inductors, but also requires large area of the chip to be allocated exclusively for this purpose. In an active inductance the value of inductance is usually independent of the size of the inductor. In addition, the passive inductors (unlike active ones) should be placed physically far from each other to prevent cross-talk between them. Never the less, the active inductors have few draw backs of their own. One of such drawbacks is their linear operating range. The linear operating range of an active inductor is limited by design. For the inductors shown in Fig. 4.5 the operating power range is roughly one third of the saturation current of the FET times the voltage difference between the gate and drain of the transistor.[29]

Here, let's review briefly the inductors presented in Fig. 4.5.[28-29] In Fig. 4.5a the first of these series of active inductors is presented. This is the simplest from of active inductor shown in this figure.[28] The impedance of this circuit can be calculated as:

$$Z = \frac{1 + j\omega C_{gs1} R_{ext}}{g_{m1} + j\omega C_{gs1} - C_{gs2} + \omega^2 C_{gs2}\left(\frac{C_{gs1} C_{gs2}}{g_{m1} g_{m2}}\right)} \qquad \text{Eq. 4.1}$$

So, if we assume the two transistors are the same, we can write[28]:

$$Z = \frac{1 + j\omega C_{gs} R_{ext}}{g_{m1} + j\omega C_{gs}\left(\frac{\omega C_{gs}}{g_m}\right)^2} \qquad \text{Eq. 4.2}$$

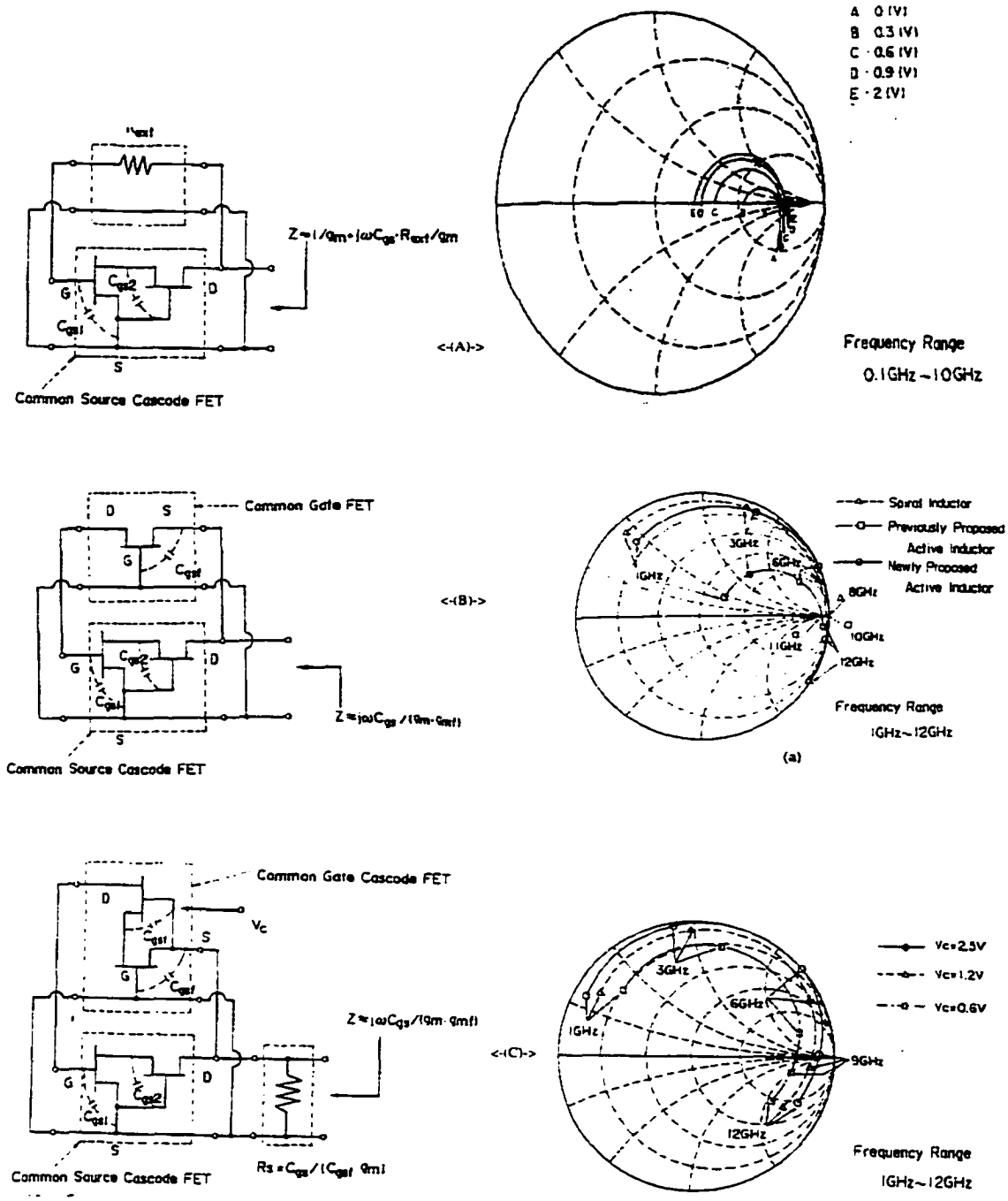


Fig. 4.5. The proposed active inductors.[28-29]

Now, if the intention is to realize an active inductor, then $g_{m1} >> j\omega.C_{gs}(\frac{\omega C_{gs}}{g_m})^2$ condition should hold. In that case $Z = \frac{1 + j\omega C_{gs} R_{ext}}{g_m}$. This means the resistivity of the inductor is equal to $r = \frac{1}{g_m}$ and its reactance will be equal to $G = j\omega \frac{C_{gs} R_{ext}}{g_{m1}}$.

The disadvantages of the inductor shown in Fig. 4.5a are the associated resistance (r) and the fact that the resistor (R_{ext}) takes a large space on the chip. To overcome these problems the circuits in Fig. 4.5b and Fig. 4.5c have been proposed.[29] In Fig. 4.5b a transistor has replaced the original R_{ext}. The admittance Y of this circuit is given as:[29]

$$Y = g_{mf}\left[1 - \frac{C_{gs2} g_{m1}}{C_{gs1} g_{m2}}\right] + \frac{g_{m1} g_{mf}}{j\omega C_{gs1}} \qquad \text{Eq. 4.3}$$

where, subscript 1,2, and f refers to first, second and the feedback transistor. Now, it is interesting to note that if the first and the second transistor are similar, the "theoretical" resistivity of the circuit goes to zero. This leaves a purely inductive component:

$$Z = j\omega \frac{C_{gs}}{g_m g_{mf}} \qquad \text{Eq. 4.4}$$

Of course, in reality there is always a small value of resistance associated with this circuit, as it can be observed from measured values plotted on the smith chart next to this figure.

In case of Fig. 4.5c a common-gate cascade FET is replaced the feedback resistor of Fig. 4.5a. This configuration make it possible to have a negative resistor be associated with this circuit:[29]

$$Y = -g_m \frac{C_{gsf}}{C_{gs}} + \frac{1}{j\omega(\frac{C_{gs}}{g_m g_{mf}})} \qquad \text{Eq. 4.5}$$

If this circuit is designed in such a way that a small theoretical negative resistance to be associated with it, the actual circuit will have zero net resistance. This means inductors with very high Q can be produced. However, larger values of negative resistance could make the circuit unstable.

4.2. 3DI Microwave Technology

Finally, the issue of most compatible microwave technology with 3DI requirements should be addressed here. As previously demonstrated in chapter 2, in order to eliminate the cross-talk between the layers a shield layer should be placed between adjacent layers in 3DI technology.[30] This makes the microwave layer sandwiched between these two shield layers (one on the top and one on the bottom) very similar to stripline technology. Therefore, a closer look at this technology and its possible application for 3DI technology is in order.

Stripline was originally developed for solid state microwave circuit boards. This configuration encloses a microwave circuit board inside a metallic (conductive enclosure); therefore, eliminating any interface or cross talk between the circuit and the environment around it. Normally in this configuration it is assumed that the distance between the transmission line and the top or the bottom conductor is equal. The distance between the ground plates is b and the width of the transmission line is designed by W, as shown if Fig. 4.6. Stripline supports TEM mode of transmission. This eliminates the dispersion phenomenon associated with wave guides. A cautionary note is in order here, similar to coaxial lines, the stripline can support TM and TE modes as well. These modes should be avoided, because of the dispersion phenomenon associated with them. In order to avoid these modes usually the distance between the ground plates should be kept to less than $\frac{\lambda}{4}$.[31]

Even though, the exact analysis of striplines is a complicated issue; a few simplification can make this task more manageable. First, it is assumed that only TEM mode is present and the designer took percussion to avoid TE and TM modes. This assumption makes

it possible to determine the important characteristics of the circuit, such as propagation constant and characteristic impedance, by electrostatic analysis. This is done using conformal mapping approach.[32] Even so, the procedure and results of this method are very complicated. Therefore, approximate expression that produce very close results is used for design purposes. These designs are later perfected using computer analysis and real measurement. For example, the characteristic impedance of the lines in stripline can be approximated as:[32-33]

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{W_c + 0.441b} \qquad \text{Eq. 4.6}$$

where b is the distance between the top and bottom grounded conductor, W_C is the effective width of the center conductor that is calculated from the normal width of conductor W using following formula:

$$\frac{W_c}{b} = \frac{W}{b} \begin{cases} 0 & \text{for} \frac{w}{b} > 0.35 \\ (0.35 - \frac{w}{b})^2 & \text{for} \frac{w}{b} < 0.35 \end{cases} \qquad \text{Eq. 4.7}$$

Similarly, if the width of line for given characteristic impedance is to be determined: one might use the following:

$$x = \frac{30\pi}{\sqrt{\varepsilon_r} Z_o} - 0.441 \qquad \text{Eq. 4.8}$$

$$\frac{W}{b} = \begin{cases} x & \text{for} \quad \sqrt{\varepsilon_r} Z_o < 120 \\ 0.85 - \sqrt{0.6 - x} & \text{for} \quad \sqrt{\varepsilon_r} Z_o > 120 \end{cases} \qquad \text{Eq. 4.9}$$

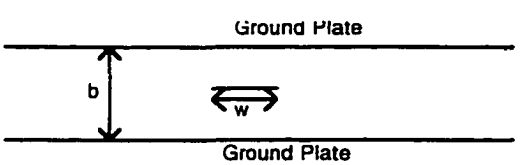


Fig. 4.6. Stripline transmission lines.

5. PRACTICAL CONSIDERATIONS IN CHOICE OF DEVICE MATERIAL

The theory of our proposed device is outlined in chapter 1. Let us reflect on the practical considerations in choosing the material for the source, drain and the gate of the n and p type semiconductor transistor.

Due to the fact that most metals diffuse inside the semiconductor at high temperatures, metal-silicides instead of pure metals should be utilized for the gate region. Unlike metals, metal-silicides are stoichiometric compounds and have negligible diffusion coefficient in semiconductors. Note that chemical bond should be broken for stoichiometric compounds to diffuse inside silicon, and breaking such chemical bond requires large amount of energy. Even though, it is desirable to use metal-silicide for source and drain too, it should be noted that there are very few metal-silicides that are suited for source and drain ohmic contact as explained below:

As explained previously, in n type material for Schottky barrier to have ohmic characteristics the Φm (metal work function) should be less than Φs (semiconductor work function). Examining various metal-silicides, the following silicides are found to be good candidates for ohmic contact and can be used for source and drain of the n type device:[34]

metal-silicide	barrier height (with n type silicon)
Ysi2	0.39(ev)
DySi2	0.37(ev)
HoSi2	0.37(ev)
GdSi2	0.37(ev)
ErSi2	0.39(ev)

In p type material for Schottky barrier to have ohmic characteristics, the Φm should be greater than Φs . Examining various metal-silicides, following silicides are found to be good candidates for ohmic contact and can be used for source and drain of the p type device:

metal-silicide	barrier height (with p type silicon)
PtSi	0.255(ev)
IrSi	0.195(ev)
Ir2Si3	0.275(ev)
IrSi3	0.185(ev)

Using the barrier heights given above, one can calculate maximum doping concentration of p and n type devices, as shown bellow. For p type device's Ohmic Contact:

$$\Phi m > \Phi s \quad \text{Eq. 5.1}$$

$$Xs + Eg - \Phi bp > Xs + Eg - (EF - EV) \quad \text{Eq. 5.2}$$

$$-\Phi bp > -(EF - EV) \quad \text{Eq. 5.3}$$

$$-\Phi bp > EV - EF \quad \text{Eq. 5.4}$$

$$-\Phi bp > KT \, Ln(\frac{N_A}{N_V}) \quad \text{Eq. 5.5}$$

$$NA < NV \exp(\frac{-\Phi_{bp}}{KT}) \quad \text{Eq. 5.6}$$

Similarly, for n type devices' Ohmic contact:

$$\Phi m < \Phi s \quad \text{Eq. 5.7}$$

$$Xs + \Phi bn < Xs + (EC - EF) \quad \text{Eq. 5.8}$$

$$\Phi bn < EC - EF \quad \text{Eq. 5.9}$$

$$-\Phi bn > EF - EC \quad \text{Eq. 5.10}$$

$$-\Phi bn > KT \, Ln(\frac{N_D}{N_C}) \quad \text{Eq. 5.11}$$

$$ND < NC \exp(\frac{-\Phi_{bn}}{KT}) \quad \text{Eq. 5.12}$$

The resulting silicon's maximum doping concentration for various metal-silicide-silicon Ohmic contacts is shown in Table 5.1.

Table 5.1. Maximum doping concentration of the semiconductor for creation of an ohmic Schottky contact.

Silicide	Max ND (n-type) #/cm3	Max NA (p-type) #/cm3
Ysi2	$9.21X10^{12}$	na
PtSi	na	$9.64X10^{14}$
DySi2	$1.99X10^{13}$	na
IrSi	na	$9.79X10^{15}$
HoSi2	$1.99X10^{13}$	na
Ir2Si3	na	$4.45X10^{14}$
GdSi2	$1.99X10^{13}$	na
IrSi3	na	$1.44X10^{16}$
ErSi2	$9.21X10^{12}$	na

As one might observe from Table 5.1, relatively pure semiconductor is required for the n type material. Even though, in theory it is possible to deposit such semiconductor using CVD; practical problems might be significant. To solve this problem an intensive literature review was conducted. Based on this research following processes have been selected for creating ohmic contact to source and drain of our devices. Before, explaining these processes in detail let's mention that there are many suitable metal-silicide for gate including: TiSi2, VSi2, WSi2 , CoSi2.

5.1. Ohmic Contact to devices on P-type semiconductor

The Ohmic contact of Al with p type silicon is relatively well known.[35] When such a contact is annealed above the eutectic temperature (T_{eut}=577°C) a low resistivity contact is

obtained from Al/Si system. This low resistivity contact has been explained based on the fact that Al solves the Si first. Later, when silicon is regrown in this liquid-phase-epitaxy (LPE) process, this Al acts as doping agent in regrown silicon, creating a highly doped p-type silicon just underneath the contact.

It has been reported that even when anneal temperatures is kept below the eutectic temperature an ohmic contact is resulted also.[36] This phenomenon is attributed to high diffusion coefficient of Al in Si.

5.2. Ohmic Contact to Devices on n-type Semiconductor

It is astonishing to learn that many reports indicate "evaporated Al (without anneal)"[37] is sometimes used for creating ohmic contact to n type silicon, as well. However, such contacts work only for a short while; after a short period (normally few days) such contacts start behaving more and more like a rectifying contact. This phenomenon is explained on the bases of room temperature diffusion of Al inside n type Si.[37] Note that Al is a p type (acceptor) impurity in the silicon. This results in creation of a p-n junction just under the Al contact. For this reason, many people in semiconductor industry consider production of such an ohmic contact as "black art".[37] Therefore, this contact is not suited for our devices.

A recent paper from "Max-Planck-Institut fur metallforschung"[37] suggest a more practical way of creating metal-semiconductor ohmic contact for n-type silicon. Since there is no known metal that can make a practical ohmic contact with n-type of silicon, this paper suggest that such an ohmic contact to be made using a Sb-Au alloy.[37] Contact area-resistivity as low as $2x10^{-2}$ Ω–Cm^2 has been achieved by utilizing this method.

The fabrication process for creation of this contact is very simple:[37] First, proportional weights of Au and Sb are melted and alloyed together inside tungsten boat of the evaporation system. Then, 300 nm of Au/Sb(%1) is deposited on top of silicon. After this step, the wafers are annealed in Ar ambient at 350 to 500°C for 5 to 45 minutes. It should be

noted that 300 nm of Au/Sb will solve 180 nm of Si at the eutectic temperature.[37] Finally, the wafers are etched and cleaned with HF and at least an additional 1um of Au is deposited on top of these contacts.

The mechanism for formation of this ohmic contact is explained based on the phase diagram of the binary Au/Sb system.[37-38] In this system Si is deposited from an Au melt. Note that the solid solubility of Au in Si at this temperature is about 10^{12} Cm^{-3}.[37] This prevents incorporation of Au (a life time killer) into Si. More over, due to high solid solubility of Sb atoms (which are donor atoms in Si) a low contact resistance is created.

6. COMPUTER SIMULATION AND VERIFICATION

It is a known fact that in today's industry computer simulation is an important part of design and development of any new product. This is the case for semiconductor industry, as well. Computer Aided Design (CAD) tools are very important in development of any new Integrated Circuit (IC) technologies. Any modern manufacturing process for ICs includes hundreds of individual steps. CAD tools can help the engineers to verify and optimize their manufacturing process. Computer simulation can reduce the time required to develop a new idea and reduce the cost associated with the developmental part of a project. Therefore, the task of designing new process using CAD tools has mostly replaced the traditional "trial-and error" approach.[39] This approach is presented in Fig. 6.1.

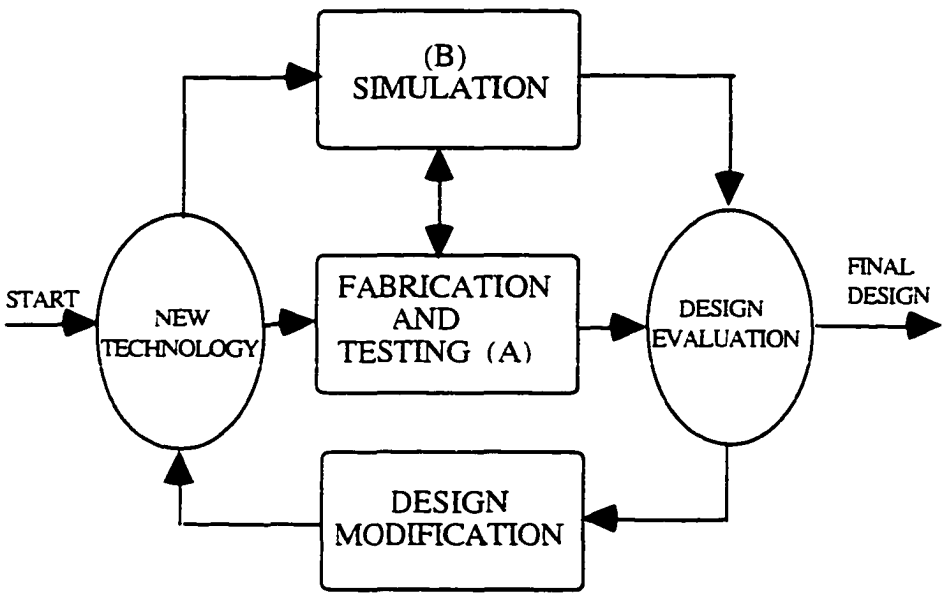


Fig. 6.1. Various ways of developing a new manufacturing process for semiconductors. Route A represents experimental approach; whereas, route B is the simulation approach (simulation here is defined as process, device, and the circuit simulation).[39]

W. Fichner of Swiss Federal Institute of Technology in his article on the virtue of simulation over the traditional "trail-and-error" approach method writes:

> The application of software tools in the development of new processes and novel device structures has become a worthwhile albeit challenging alternative to the experimental route.... Fabricating one lot in a modern process can cost considerably more than 10K dollars, consuming weeks or even months. The use of accurate simulation tools in the proper computing environment allows for comparatively inexpensive "computer experiments".[40]

Here it should be noted that process simulation encompasses all aspects of IC fabrication, as shown in Fig. 6.2. This includes process simulation, device simulation, circuit simulation, and electromagnetic simulation. Of course, there are many good software packages available for simulation of circuits and devices. SUPREM III, a version of a popular fabrication simulator in electrical engineering industry, will be utilized in this study to simulate the manufacturing process. Moreover, computer simulation will be employed in order to analyze the our device. Valuable insights in the physics of the process can be gained by analyzing these results.

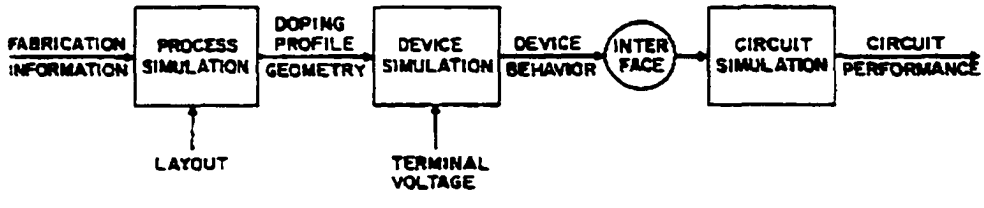


Fig. 6.2. Several sub-simulator of a process simulator.[39]

6.1. Simulation of the fabrication process using SUPREM III

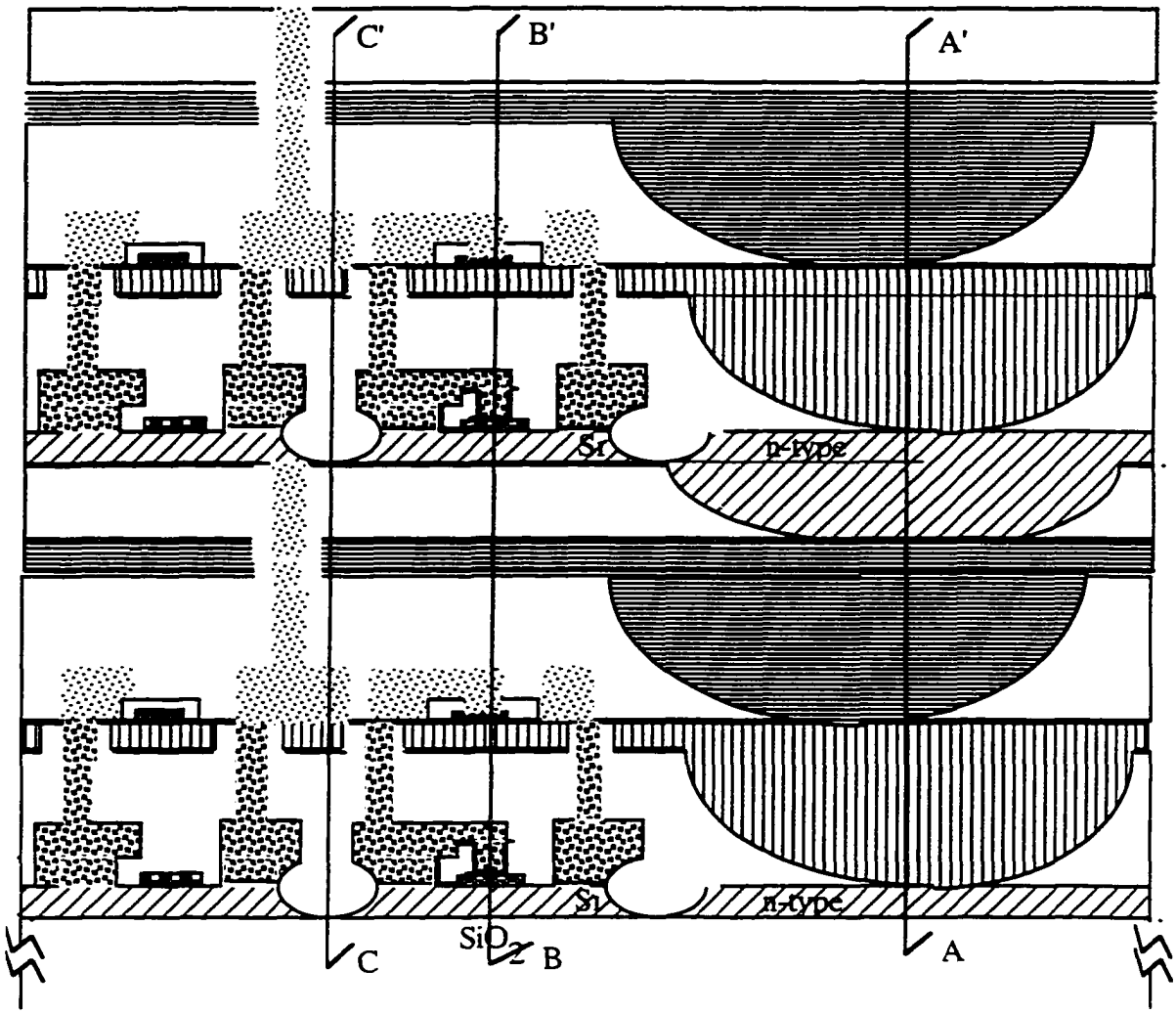
SUPREM is extensively used in simulation of fabrication process in the semiconductor industry. Today, no one even think of fabricating semiconductors without verifying it's fabrication process first by SUPREM or some other form of computer simulation. Therefore, simulation is the first step in verification of this work as well.

The version of SUPREM that we utilized to verify our process (SUPREM III) only simulate one dimensional structures. Simulating the fabrication process in one dimension has many advantages, including lower demand on computational resources. More over if several cross sections is to be chosen correctly, the whole process can be verified.

Therefore, three cross sections from Fig. 4.20 (AA', BB', CC') is chosen and simulated by SUPREM. These cross sections are shown in Fig. 6.3. The simulation listing for each of these cross sections are listed in Fig. 6.4, Fig. 6.5, and Fig. 6.6. The one dimensional profile of the semiconductor prepared by the simulation program for each cross section is shown in Figs. 6.7 to 6.9.

Note that in Figs. 6.7 to 6.9 the distance is measured from surface of the semiconductor. Therefore, the first layer is positioned at deeper distance than the second layer.

As it can be seen from the listings, the SUPREM program used for simulation of these cross sections is developed by Technology Modeling Associates, Inc. It is version P, Revision 9002 of SUPREM program that is developed by this company. This information is presented here because different versions of SUPREM may produce slightly different results depending on their internal procedures to simulate the process. More over, the syntax of this version SUPREM differs slightly from syntax used by the version developed Stanford University. However, the final results should be the same in large part, regardless of what version of SUPREM is used for simulating the process.



Gate metal (for n-type semiconductor)
Si (n-type)
SiO_2
Source and Drain Metal (for n-type semiconductor)
Si (p-type)
Source and Drain Metal (for p-type semiconductor)
Gate metal (for p-type semiconductor)
Highly doped n-type semiconductor

Fig. 6.3. The cross sections of two stacked layers chosen for computer simulation.

```
*************************************************************
***                      SUPREM-3                         ***
***               Version P, Revision 9002                ***
***    Copyright (C) 1985,1986,1987,1988,1989,1990        ***
***        Technology Modeling Associates, Inc.           ***
***                 All Rights Reserved                   ***
***                                                       ***
***          Licensed to Iowa State University            ***
***                 Serial # 0155401845                   ***
*************************************************************

                      16-Aug-95 15:54:10


     Statements input from file aa.sup


    1... Title 3DI simulationfor AA cross section
    2... $ Let's initilize the substrate to a <100> regular silicon wafer
    3... $with doping density consentration of 4X10^14 Phosphourous
Atoms/Cm3
    4... Initialize <100> silicon, phosphor=5e14, Thickness=3.0 dx=0.1
    5... $let's grow a layer of oxide on top of this wafer by LPCVD method
    6... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
    7... Deposition Thickness=2 Oxide DX=0.1 temperat=500
    8... $ let's etch the oxide to create a seeding window
    9... etch oxide all
   10... $Now let's grow a layer of poly-silicon top this layer
   11... $Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
   12... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
     ... + Phosphor=5e14
   13... $Now it is time to deposit gate metal using Following reaction
using LPCVD
   14... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
   15... $Before doing this we have to define the Tungsten metal for the
Suprem
   16... $using Material statement
   17... Material Mater.7 Name=Tungsten dx.defau=0.1 N.specie=1
     ... + Density=19.3   AT.WT.1=183.85    AT.num.1=74    Abund.1=1
     ... + Conducto  work.fun=4.6
   18... Deposition Mater.7 thickness=1 dx=0.1
   19... $ we have to etch all the Tungsten from this location
   20... Etch Mater.7 ALL
   21... $let's grow a layer of oxide on top of this wafer by LPCVD method
   22... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
   23... Deposition Thickness=2 Oxide DX=0.1 temperat=500
   24... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
   25... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
   26... $ Followed by heating step that results to reaction below:
```

Fig. 6.4 SUPREM code to analyze AA' cross section

```
  27... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  28... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  29... Diffusion NITROGEN Temperat=300 time=60
  30... $ Now let's etch the aluminum away for this region (AA')
  31... Etch Aluminum All
  32... $let's grow a layer of oxide on top of this wafer by LPCVD method
  33... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  34... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  35... $ Now we have to etch the oxide away to creat seeding window for
next
  36... $ layer
  37... Etch Oxide All
  38... $ Now let's grow a layer of poly-silicon top this layer
  39... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  40... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
  41... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
  42... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  43... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  44... $ we have to etch all the Tungsten from this location
  45... Etch Mater.7 ALL
  46... $let's grow a layer of oxide on top of this wafer by LPCVD method
  47... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  48... Deposition Thickness=2 Oxide DX=0.1 temperat=500
  49... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  50... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  51... $ Followed by heating step that results to reaction below:
  52... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  53... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  54... Diffusion NITROGEN Temperat=300 time=60
  55... $ Now let's etch the aluminum away for this region (AA')
  56... Etch Aluminum All
  57... $let's grow a layer of oxide on top of this wafer by LPCVD method
  58... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  59... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  60... $ Now we have to etch the oxide away to creat seeding window for
next
  61... $ layer
  62... Etch Oxide All
  63... $ Now let's grow a layer of poly-silicon top this layer
  64... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  65... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
  66... $let's grow a layer of oxide on top of this wafer by LPCVD method
  67... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  68... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  69... $ Now we have to etch the oxide away to creat seeding window for
next
  70... $ layer
  71... Etch Oxide All
  72... $Now let's grow a layer of poly-silicon top this layer
```

Fig. 6.4. Continued

```
  73... $Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  74... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e14
  75... $Now it is time to deposit gate metal using Following reaction
using LPCVD
  76... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  77... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  78... $ we have to etch all the Tungsten from this location
  79... etch Mater.7 ALL
  80... $let's grow a layer of oxide on top of this wafer by LPCVD method
  81... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  82... Deposition Thickness=2 Oxide DX=0.1 temperat=500
  83... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  84... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  85... $ Followed by heating step that results to reaction below:
  86... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  87... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  88... Diffusion NITROGEN Temperat=300 time=60
  89... $ Now let's etch the aluminum away for this region (AA')
  90... Etch Aluminum All
  91... $let's grow a layer of oxide on top of this wafer by LPCVD method
  92... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  93... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  94... $ Now we have to etch the oxide away to creat seeding window for
next
  95... $ layer
  96... Etch Oxide All
  97... $ Now let's grow a layer of poly-silicon on top this layer
  98... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  99... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
 100... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
 101... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
 102... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
 103... $ we have to etch all the Tungsten from this location
 104... etch Mater.7 ALL
 105... $let's grow a layer of oxide on top of this wafer by LPCVD method
 106... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
 107... Deposition Thickness=2 Oxide DX=0.1 temperat=500
 108... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
 109... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
 110... $ Followed by heating step that results to reaction below:
 111... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
 112... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
 113... Diffusion NITROGEN Temperat=300 time=60
 114... $ Now let's etch the aluminum away for this region (AA')
 115... Etch Aluminum All
 116... $let's grow a layer of oxide on top of this wafer by LPCVD method
 117... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
```

Fig. 6.4. Continued

```
 118... Deposition Thickness=10 Oxide DX=0.1 temperat=500
 119... $ Now we have to etch the oxide away to creat seeding window for
next
 120... $ layer
 121... Etch Oxide All
 122... $ Now let's grow a layer of poly-silicon top this layer
 123... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
 124... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
 125... $ this conclude two complete circuit layer each having a P-layer, a
n-layer
 126... $ and a shield layer
 127... Print Layer
 128... plot active acceptor
 129... plot active donor add color=2 pause


 Input line #   4
 Coefficient data group read
 File: \tma\s3_9002\library\s3cof0
 Date: 18-Apr-95 09:53:40
 Documentation from data file:

 SUPREM-3 Revision 8834 coefficient initialization
 Modifications for new oxidation coefficients


 Warning number   45 detected in line number  29
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  54
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  88
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number 113
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.
1
 3DI simulationfor AA cross section
 and a shield layer

 Material layer information
 Input line # 127
```

Fig. 6.4. Continued

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	polysilicon	6.0000	.1000	5.00	909	969	.0019
1	silicon	3.0000	.1000	.00	970	1000	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	boron	phosphorus
2	9.9988E-01	9.9994E-01

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	1.0000E+16	1.0000E+16	1.0000E+16	1.0000E+16
1	1.4750E+11	1.4750E+11	1.4750E+11	1.4750E+11
sum	1.0000E+16	1.0000E+16	1.0000E+16	1.0000E+16

Integrated Dopant (#/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
2	9.5000E+10	9.5000E+10	1.0000E+16	1.0000E+16
1	0.0000E+00	0.0000E+00	1.4750E+11	1.4750E+11
sum	9.5000E+10	9.5000E+10	1.0000E+16	1.0000E+16

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
2	5	n	.0000	1.1000	5.0000E+15	5.0000E+15
2	4	p	1.1000	2.0016	4.2542E+10	4.5038E+10
2	3	n	2.0016	4.1000	5.0000E+15	5.0000E+15
2	2	p	4.1000	5.0016	4.2541E+10	4.5038E+10
2	1	n	5.0016	6.0000	4.9960E+10	5.2381E+10
1	1	n	.0000	3.0000	1.4750E+11	1.4750E+11

*** END SUPREM-3 ***

Fig. 6.4. Continued

```
*************************************************************
***                        SUPREM-3                       ***
***                  Version P, Revision 9002             ***
***    Copyright (C) 1985,1986,1987,1988,1989,1990        ***
***         Technology Modeling Associates, Inc.          ***
***                  All Rights Reserved                  ***
***                                                       ***
***          Licensed to Iowa State University            ***
***                  Serial # 0155401845                  ***
*************************************************************

                        17-Aug-95 17:17:10


     Statements input from file bb.sup


    1... Title 3DI simulationfor BB' cross section
    2... $ We start simulation from the 1st recrystallized polysilicon layer
    3... $ Let's initilize the substrate to a <100> regular silicon wafer
    4... $with doping density consentration of 4X10^14 Phosphourous
Atoms/Cm3
    5... $Initialize <100> silicon, phosphor=5e14, Thickness=3.0 dx=0.2
    6... $$let's grow a layer of oxide on top of this wafer by LPCVD method
    7... $$This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
    8... $Deposition Thickness=2 Oxide dx=0.2 temperat=500
    9... $$Now let's grow a layer of poly-silicon top this layer
   10... $$Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
   11... $Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-
3
   12... $+ Phosphor=5e14
   13... Initialize <100> silicon, Phosphor=5e14, thickness=1
   14... $Now it is time to deposit gate metal using Following reaction
using LPCVD
   15... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
   16... $Before doing this we have to define the Tungsten metal for the
Suprem
   17... $using Material statement
   18... Material Mater.7 Name=Tungsten dx.defau=0.1 N.specie=1
     ... + Density=19.3   AT.WT.1=183.85    AT.num.1=74    Abund.1=1
     ... + Conducto  work.fun=4.6
   19... Deposition thickness=1 Mater.7 dx=0.2 Temperat=300 Pressre=1.31e-3
   20... $ let's grow a layer of oxide on top of this layer by LPCVD method
   21... $ This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
   22... Deposition Thickness=2 Oxide dx=0.2 temperat=500
   23... $ Let's etch this oxide layer to open for a via
   24... Etch oxide all
   25... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
   26... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
```

Fig 6.5. SUPREM code to analyze BB' cross section

```
  27... $ Followed by heating step that results to reaction below:
  28... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  29... Deposition thickness=1 Aluminum dx=0.2 Temperat=100
  30... Diffusion NITROGEN Temperat=300 time=60
  31... $let's grow a layer of oxide on top of this wafer by LPCVD method
  32... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  33... Deposition Thickness=10 Oxide dx=0.2 temperat=500
  34... $============================== end of layer 1 ====================
  35... $ Now let's grow a layer of poly-silicon top this layer
  36... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  37... Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
  38... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
  39... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  40... Deposition thickness=1 Mater.7 dx=0.2 Temperat=300 Pressre=1.31e-3
  41... $let's grow a layer of oxide on top of this wafer by LPCVD method
  42... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  43... Deposition Thickness=2 Oxide dx=0.2 temperat=500
  44... $ Let's Etch the Oxide to provide for via
  45... Etch oxide all
  46... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  47... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  48... $ Followed by heating step that results to reaction below:
  49... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  50... Deposition thickness=1 Aluminum dx=0.2 Temperat=100
  51... Diffusion NITROGEN Temperat=300 time=60
  52... $let's grow a layer of oxide on top of this wafer by LPCVD method
  53... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  54... Deposition Thickness=10 Oxide dx=0.2 temperat=500
  55... $============================== end of layer 2 ====================
  56... $ Now let's grow a layer of poly-silicon top this layer
  57... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  58... Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
  59... $let's grow a layer of oxide on top of this wafer by LPCVD method
  60... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  61... Deposition Thickness=10 Oxide dx=0.2 temperat=500
  62... $============================== end of layer 3 ====================
  63... $Now let's grow a layer of poly-silicon top this layer
  64... $Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  65... Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e14
  66... $Now it is time to deposit gate metal using Following reaction
using LPCVD
  67... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  68... Deposition thickness=1 Mater.7 dx=0.2 Temperat=300 Pressre=1.31e-3
  69... $ let's grow a layer of oxide on top of this layer by LPCVD method
  70... $ This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  71... Deposition Thickness=2 Oxide dx=0.2 temperat=500
  72... $ Let's etch this oxide layer to open for a via
```

Fig 6.5. Continued.

```
  73... Etch oxide all
  74... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  75... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  76... $ Followed by heating step that results to reaction below:
  77... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  78... Deposition thickness=1 Aluminum dx=0.2 Temperat=100
  79... Diffusion NITROGEN Temperat=300 time=60
  80... $let's grow a layer of oxide on top of this wafer by LPCVD method
  81... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  82... Deposition Thickness=10 Oxide dx=0.2 temperat=500
  83... $============================== end of layer 4 ====================
  84... $ Now let's grow a layer of poly-silicon top this layer
  85... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  86... Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
  87... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
  88... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  89... Deposition thickness=1 Mater.7 dx=0.2 Temperat=300 Pressre=1.31e-3
  90... $let's grow a layer of oxide on top of this wafer by LPCVD method
  91... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  92... Deposition Thickness=2 Oxide dx=0.2 temperat=500
  93... $ Let's Etch the Oxide to provide for via
  94... Etch oxide all
  95... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  96... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  97... $ Followed by heating step that results to reaction below:
  98... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  99... Deposition thickness=1 Aluminum dx=0.2 Temperat=100
 100... Diffusion NITROGEN Temperat=300 time=60
 101... $let's grow a layer of oxide on top of this wafer by LPCVD method
 102... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
 103... Deposition Thickness=10 Oxide dx=0.2 temperat=500
 104... $============================== end of layer 5 ====================
 105... $ Now let's grow a layer of poly-silicon top this layer
 106... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
 107... Deposition Thickness=1 POLYSIL dx=0.2 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
 108... $let's grow a layer of oxide on top of this wafer by LPCVD method
 109... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
 110... Deposition Thickness=10 Oxide dx=0.2 temperat=500
 111... $============================== end of layer 6 ====================
 112... $ this conclude two complete circuit layer each having a P-layer, a
n-layer
 113... $ and a shield layer
 114... Print Layer
 115... plot chemical
 116... plot active acceptor add color=3
 117... plot active donor add color=2 pause
```

Fig 6.5. Continued.

```
 Input line #  13
 Coefficient data group read
 File: \tma\s3_9002\library\s3cof0
 Date: 18-Apr-95 09:53:40
 Documentation from data file:

 SUPREM-3 Revision 8834 coefficient initialization
 Modifications for new oxidation coefficients


 Warning number   45 detected in line number  30
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  51
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  79
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number 100
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.
1
 3DI simulationfor BB' cross section
 and a shield layer

 Material layer information
 Input line # 114


 layer  material      thickness    dx      xdx  top bottom  orientation
  no.                    (um)     (um)    (um) node  node  or grain size
  20    oxide          10.0000    .2000    .00  516   566
  19    polysilicon     1.0000    .2000    .00  567   572        .0010
  18    oxide          10.0000    .2000    .00  573   623
  17    aluminum        1.0000    .2000    .00  624   629
  16    Tungsten        1.0000    .2000    .00  630   635
  15    polysilicon     1.0000    .2000    .00  636   641        .0013
  14    oxide          10.0000    .2000    .00  642   692
  13    aluminum        1.0000    .2000    .00  693   698
  12    Tungsten        1.0000    .2000    .00  699   704
  11    polysilicon     1.0000    .2000    .00  705   710        .0015
  10    oxide          10.0000    .2000    .00  711   761
   9    polysilicon     1.0000    .2000    .00  762   767        .0017
   8    oxide          10.0000    .2000    .00  768   818
```

Fig 6.5. Continued.

7	aluminum	1.0000	.2000	.00	819	824	
6	Tungsten	1.0000	.2000	.00	825	830	
5	polysilicon	1.0000	.2000	.00	831	836	.0017
4	oxide	10.0000	.2000	.00	837	887	
3	aluminum	1.0000	.2000	.00	888	893	
2	Tungsten	1.0000	.2000	.00	894	899	
1	silicon	1.0000	.0100	.00	900	1000	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	boron	phosphorus
19	1.0000E+00	1.0000E+00
15	9.9994E-01	1.0000E+00
11	1.0000E+00	9.9988E-01
9	1.0000E+00	9.9988E-01
5	9.9982E-01	1.0000E+00

1

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
20	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
19	5.0000E+15	5.0000E+15	5.0000E+15	5.0000E+15
18	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
17	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
16	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
15	-4.5000E+10	-4.5000E+10	4.5000E+10	4.5000E+10
14	-5.0000E+09	-5.0000E+09	5.0000E+09	5.0000E+09
13	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
12	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
11	4.9839E+10	4.9839E+10	4.9839E+10	4.9839E+10
10	1.6129E+13	1.6129E+13	1.6129E+13	1.6129E+13
9	4.9677E+15	4.9677E+15	4.9677E+15	4.9677E+15
8	1.6129E+13	1.6129E+13	1.6129E+13	1.6129E+13
7	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
6	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
5	-4.5000E+10	-4.5000E+10	4.5000E+10	4.5000E+10
4	-5.0000E+09	-5.0000E+09	5.0000E+09	5.0000E+09
3	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
2	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
1	5.0000E+10	5.0000E+10	5.0000E+10	5.0000E+10
sum	1.0000E+16	1.0000E+16	1.0000E+16	1.0000E+16

Integrated Dopant (#/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
20	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
19	0.0000E+00	0.0000E+00	5.0000E+15	5.0000E+15
18	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
17	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
16	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
15	4.5000E+10	4.5000E+10	0.0000E+00	0.0000E+00

Fig 6.5. Continued.

14	5.0000E+09	5.0000E+09	0.0000E+00	0.0000E+00
13	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
12	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
11	0.0000E+00	0.0000E+00	4.9839E+10	4.9839E+10
10	0.0000E+00	0.0000E+00	1.6129E+13	1.6129E+13
9	0.0000E+00	0.0000E+00	4.9677E+15	4.9677E+15
8	0.0000E+00	0.0000E+00	1.6129E+13	1.6129E+13
7	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
6	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
5	4.5000E+10	4.5000E+10	0.0000E+00	0.0000E+00
4	5.0000E+09	5.0000E+09	0.0000E+00	0.0000E+00
3	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
2	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
1	0.0000E+00	0.0000E+00	5.0000E+10	5.0000E+10
sum	1.0000E+11	1.0000E+11	1.0000E+16	1.0000E+16

1

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
20			.0000	10.0000	0.0000E+00	0.0000E+00
19	1	n	.0000	1.0000	5.0000E+15	5.0000E+15
18			.0000	10.0000	0.0000E+00	0.0000E+00
17			.0000	1.0000	0.0000E+00	0.0000E+00
16	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
15	1	p	.0000	1.0000	4.5000E+10	4.5000E+10
14	1	p	.0000	.4000	4.9997E+09	4.9997E+09
13			.0000	1.0000	0.0000E+00	0.0000E+00
12	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
11	1	n	.0000	1.0000	4.9839E+10	4.9839E+10
10	2	n	.0000	.6000	1.6128E+08	1.6128E+08
10	1	n	9.4000	10.0000	1.6129E+13	1.6129E+13
9	1	n	.0000	1.0000	4.9677E+15	4.9677E+15
8	1	n	.0000	.6000	1.6128E+13	1.6128E+13
7			.0000	1.0000	0.0000E+00	0.0000E+00
6	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
5	1	p	.0000	1.0000	4.5000E+10	4.5000E+10
4	1	p	.0000	.6000	4.9998E+09	4.9998E+09
3			.0000	1.0000	0.0000E+00	0.0000E+00
2	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
1	1	n	.0000	1.0000	5.0000E+10	5.0000E+10

*** END SUPREM-3 ***

Fig 6.5. Continued.

```
*************************************************************
***                        SUPREM-3                       ***
***                  Version P, Revision 9002             ***
***    Copyright (C) 1985,1986,1987,1988,1989,1990        ***
***        Technology Modeling Associates, Inc.           ***
***                  All Rights Reserved                  ***
***                                                       ***
***          Licensed to Iowa State University            ***
***                  Serial # 0155401845                  ***
*************************************************************

                       17-Aug-95 17:41:44


     Statements input from file cc.sup


   1... Title 3DI simulationfor CC' cross section
   2... $ Let's initilize the substrate to a <100> regular silicon wafer
   3... $with doping density consentration of 4X10^14 Phosphourous
Atoms/Cm3
   4... Initialize <100> silicon, phosphor=5e14, Thickness=3.0 dx=0.1
   5... $let's grow a layer of oxide on top of this wafer by LPCVD method
   6... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
   7... Deposition Thickness=2 Oxide DX=0.1 temperat=500
   8... $Now let's grow a layer of poly-silicon on top this layer
   9... $Using SiH4->2H2+Si at 0.5 torr of pressure using Plasma CVD
  10... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
     ... + Phosphor=5e14
  11... $ we have to each all the polysilicon from this location
  12... etch Polysili ALL
  13... $Now it is time to deposit gate metal using Following reaction
using LPCVD
  14... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  15... $Before doing this we have to define the Tungsten metal for the
Suprem
  16... $using Material statement
  17... Material Mater.7 Name=Tungsten dx.defau=0.1 N.specie=1
     ... + Density=19.3   AT.WT.1=183.85    AT.num.1=74    Abund.1=1
     ... + Conducto  work.fun=4.6
  18... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  19... $ we have to etch all the Mater.7 from this location
  20... etch Mater.7 ALL
  21... $let's grow a layer of oxide on top of this wafer by LPCVD method
  22... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  23... Deposition Thickness=2 Oxide DX=0.1 temperat=500
  24... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  25... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
```

Fig. 6.6 SUPREM code to analyze CC' cross section

```
  26... $ Followed by heating step that results to reaction below:
  27... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  28... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  29... Diffusion NITROGEN Temperat=300 time=60
  30... $ Now let's etch the aluminum away for this region (AA')
  31... Etch Aluminum All
  32... $let's grow a layer of oxide on top of this wafer by LPCVD method
  33... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  34... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  35... $ Now let's grow a layer of poly-silicon top this layer
  36... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  37... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
  38... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
  39... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  40... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  41... $let's grow a layer of oxide on top of this wafer by LPCVD method
  42... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  43... Deposition Thickness=2 Oxide DX=0.1 temperat=500
  44... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  45... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  46... $ Followed by heating step that results to reaction below:
  47... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  48... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  49... Diffusion NITROGEN Temperat=300 time=60
  50... $let's grow a layer of oxide on top of this wafer by LPCVD method
  51... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  52... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  53... $ Now let's grow a layer of poly-silicon top this layer
  54... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  55... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
  56... $let's grow a layer of oxide on top of this wafer by LPCVD method
  57... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  58... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  59... $ Now let's grow a layer of poly-silicon on top this layer
  60... $ Using SiH4->2H2+Si at 0.5 torr of pressure using Plasma CVD
  61... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e14
  62... $ we have to each all the polysilicon from this location
  63... etch Polysili ALL
  64... $Now it is time to deposit gate metal using Following reaction
using LPCVD
  65... $2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  66... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  67... $ we have to etch all the Mater.7 from this location
  68... etch Mater.7 ALL
  69... $let's grow a layer of oxide on top of this wafer by LPCVD method
  70... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  71... Deposition Thickness=2 Oxide DX=0.1 temperat=500
```

Fig. 6.6 Continued.

```
  72... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  73... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  74... $ Followed by heating step that results to reaction below:
  75... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  76... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  77... Diffusion NITROGEN Temperat=300 time=60
  78... $ Now let's etch the aluminum away for this region (AA')
  79... Etch Aluminum All
  80... $let's grow a layer of oxide on top of this wafer by LPCVD method
  81... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  82... Deposition Thickness=10 Oxide DX=0.1 temperat=500
  83... $ Now let's grow a layer of poly-silicon top this layer
  84... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
  85... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Boron=5e14
  86... $ Now it is time to deposit gate metal using Following reaction
using LPCVD
  87... $ 2WF6+3Si->3SiF4+2W at 300'C& 0.64 torr
  88... Deposition thickness=1 Mater.7 dx=0.1 Temperat=300 Pressre=1.31e-3
  89... $let's grow a layer of oxide on top of this wafer by LPCVD method
  90... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
  91... Deposition Thickness=2 Oxide DX=0.1 temperat=500
  92... $ Let's deposit Aluminum using LPCVD for the source and drian
contacts using
  93... $ [(CH3)2CH-CH2]3AL->[(CH3)2 CH-CH2]2 ALH +(CH3)2C=CH2 at 100 'C
  94... $ Followed by heating step that results to reaction below:
  95... $ [(CH3)2CH-CH2]2 ALH -> Al+ 3/2 H2 + 2(CH3)C=CH2
  96... Deposition thickness=1 Aluminum dx=0.1 Temperat=100
  97... Diffusion NITROGEN Temperat=300 time=60
  98... $let's grow a layer of oxide on top of this wafer by LPCVD method
  99... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
 100... Deposition Thickness=10 Oxide DX=0.1 temperat=500
 101... $ Now let's grow a layer of poly-silicon top this layer
 102... $ Using SiH4->2H2+Si at 0.5 torrof pressure using Plasma CVD
 103... Deposition Thickness=1 POLYSIL dx=0.1 Temperat=300 Pressure=1.31e-3
    ... + Phosphor=5e19
 104... $let's grow a layer of oxide on top of this wafer by LPCVD method
 105... $This can be done by: SiH4+O2->SiO2+2H2 at 500 'C
 106... Deposition Thickness=10 Oxide DX=0.1 temperat=500
 107... $ this conclude two complete circuit layer each having a P-layer, a
n-layer
 108... $ and a shield layer
 109... Print Layer
 110... plot active acceptor
 111... plot active donor add color=2 pause
```

Fig. 6.6 Continued.

```
 Input line #   4
 Coefficient data group read
 File: \tma\s3_9002\library\s3cof0
 Date: 18-Apr-95 09:53:40
 Documentation from data file:

 SUPREM-3 Revision 8834 coefficient initialization
 Modifications for new oxidation coefficients


 Warning number   45 detected in line number  29
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  49
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  77
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.

 Warning number   45 detected in line number  97
 The temperature specified was less than 800 degrees Celsius.
 The default diffusion and oxidation coefficients are not reliable
 below this temperature.
1
 3DI simulationfor CC' cross section
 and a shield layer

 Material layer information
 Input line # 109


 layer  material      thickness    dx       xdx   top  bottom  orientation
  no.                    (um)     (um)     (um) node   node  or grain size
  16    oxide          10.0000    .1000     .00  175    275
  15    polysilicon     1.0000    .1000     .00  276    286        .0010
  14    oxide          10.0000    .1000     .00  287    387
  13    aluminum        1.0000    .1000     .00  388    398
  12    oxide           2.0000    .1000     .00  399    419
  11    Tungsten        1.0000    .1000     .00  420    430
  10    polysilicon     1.0000    .1000     .00  431    441        .0013
   9    oxide          22.0000    .1000   12.00  442    662
   8    polysilicon     1.0000    .1000     .00  663    673        .0017
   7    oxide          10.0000    .1000     .00  674    774
   6    aluminum        1.0000    .1000     .00  775    785
   5    oxide           2.0000    .1000     .00  786    806
   4    Tungsten        1.0000    .1000     .00  807    817
```

Fig. 6.6 Continued.

3	polysilicon	1.0000	.1000	.00	818	828	.0017
2	oxide	14.0000	.1000	12.00	829	969	
1	silicon	3.0000	.1000	.00	970	1000	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	boron	phosphorus
15	1.0000E+00	1.0000E+00
10	9.9994E-01	1.0000E+00
8	1.0000E+00	9.9988E-01
3	9.9982E-01	1.0000E+00

Integrated Dopant (#/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
16	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
15	5.0000E+15	5.0000E+15	5.0000E+15	5.0000E+15
14	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
13	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
12	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
11	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
10	-4.7500E+10	-4.7500E+10	4.7500E+10	4.7500E+10
9	8.0618E+12	8.0618E+12	8.0668E+12	8.0668E+12
8	4.9839E+15	4.9839E+15	4.9839E+15	4.9839E+15
7	8.0645E+12	8.0645E+12	8.0645E+12	8.0645E+12
6	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
5	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
4	1.3100E-07	1.3100E-07	1.3100E-07	1.3100E-07
3	-4.7500E+10	-4.7500E+10	4.7500E+10	4.7500E+10
2	-2.4904E+09	-2.4904E+09	2.5095E+09	2.5095E+09
1	1.4999E+11	1.4999E+11	1.4999E+11	1.4999E+11
sum	1.0000E+16	1.0000E+16	1.0000E+16	1.0000E+16

1

Integrated Dopant (#/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
16	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
15	0.0000E+00	0.0000E+00	5.0000E+15	5.0000E+15
14	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
13	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
12	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
11	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
10	4.7500E+10	4.7500E+10	0.0000E+00	0.0000E+00
9	2.5000E+09	2.5000E+09	8.0643E+12	8.0643E+12
8	0.0000E+00	0.0000E+00	4.9839E+15	4.9839E+15
7	0.0000E+00	0.0000E+00	8.0645E+12	8.0645E+12
6	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
5	0.0000E+00	0.0000E+00	0.0000E+00	0.0000E+00
4	0.0000E+00	0.0000E+00	1.3100E-07	1.3100E-07
3	4.7500E+10	4.7500E+10	0.0000E+00	0.0000E+00

Fig. 6.6 Continued.

2	2.5000E+09	2.5000E+09	9.5070E+06	9.5070E+06
1	0.0000E+00	0.0000E+00	1.4999E+11	1.4999E+11
sum	1.0000E+11	1.0000E+11	1.0000E+16	1.0000E+16

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
16			.0000	10.0000	0.0000E+00	0.0000E+00
15	1	n	.0000	1.0000	5.0000E+15	5.0000E+15
14			.0000	10.0000	0.0000E+00	0.0000E+00
13			.0000	1.0000	0.0000E+00	0.0000E+00
12			.0000	2.0000	0.0000E+00	0.0000E+00
11	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
10	1	p	.0000	1.0000	4.7500E+10	4.7500E+10
9	2	p	.0000	.3000	2.5023E+09	2.5023E+09
9	1	n	21.7000	22.0000	8.0568E+12	8.0568E+12
8	1	n	.0000	1.0000	4.9839E+15	4.9839E+15
7	1	n	.0000	.3000	8.0648E+12	8.0648E+12
6			.0000	1.0000	0.0000E+00	0.0000E+00
5			.0000	2.0000	0.0000E+00	0.0000E+00
4	1	n	.0000	1.0000	1.3100E-07	1.3100E-07
3	1	p	.0000	1.0000	4.7500E+10	4.7500E+10
2	2	p	.0000	.3000	2.5008E+09	2.5008E+09
2	1	n	13.7000	14.0000	9.5038E+06	9.5040E+06
1	1	n	.0000	3.0000	1.4999E+11	1.4999E+11

*** END SUPREM-3 ***

Fig. 6.6 Continued.

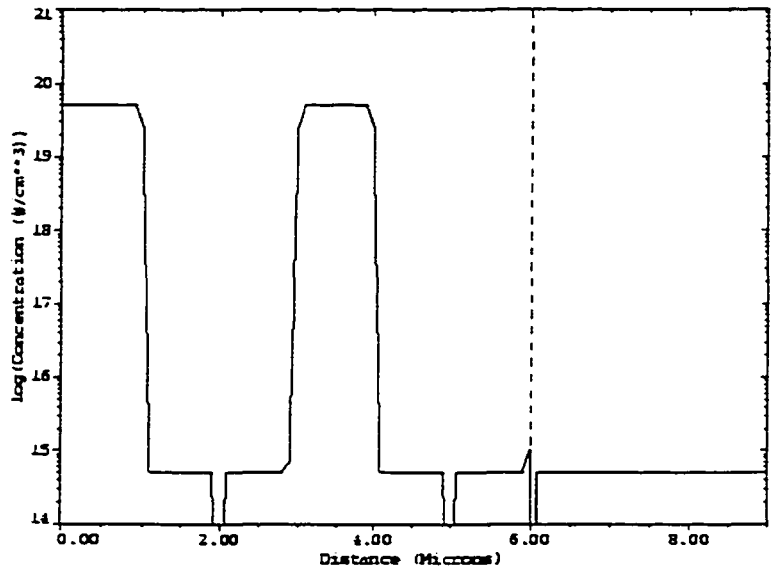


Fig. 6.7 The AA cross section generated by SUPREM

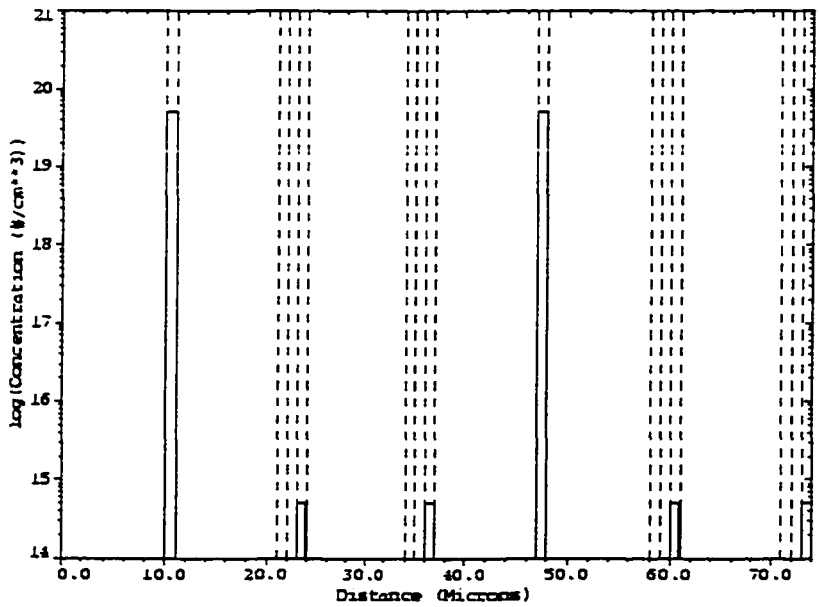


Fig. 6.8 The BB' cross section generated by SUPREM

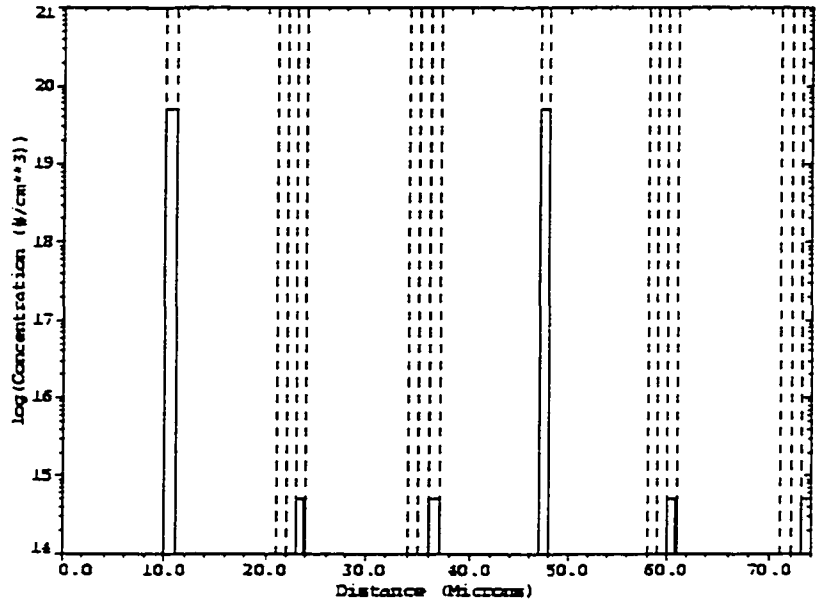


Fig. 6.9. The CC' cross section generated by SUPREM

6.3. Verification of the device using computer simulations

Although, we calculated the work equations of the proposed device in closed form; computer simulation of the gate semiconductor region may provide us better insight into the device.

The equation that governs this system are:

$$\nabla^2\Phi = -\frac{\rho}{\varepsilon} \qquad \text{Eq. 6.1}$$

$$\rho = q(p - n + \Gamma) \qquad \text{Eq. 6.2}$$

$$J_p = qD_p\frac{\partial p}{\partial x} + q\mu_p p\frac{\partial \Phi}{\partial x} \qquad \text{Eq. 6.3}$$

$$J_n = -qD_n\frac{\partial n}{\partial x} + q\mu_n n\frac{\partial \Phi}{\partial x} \qquad \text{Eq. 6.4}$$

$$J = J_n + J_p \qquad \text{Eq. 6.5}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\frac{\partial J_p}{\partial x} - R \qquad \text{Eq. 6.6}$$

$$\frac{\partial n}{\partial t} = -\frac{1}{q}\frac{\partial J_n}{\partial x} - R \qquad \text{Eq. 6.7}$$

In the above set of equations n and p are respectively the electron and hole concentrations, Γ is the net concentration of impurity atoms, and the R is the steady state recombination factor.

Utilizing Finite Difference Method (FDM)[41] this sets of equations can be solved numerically.[42-45] This process is explained in detail in Figs 6.10 to 6.17. Also, Fig. 6.18 and 6.19 present PASCAL programs that coded these algorithms.

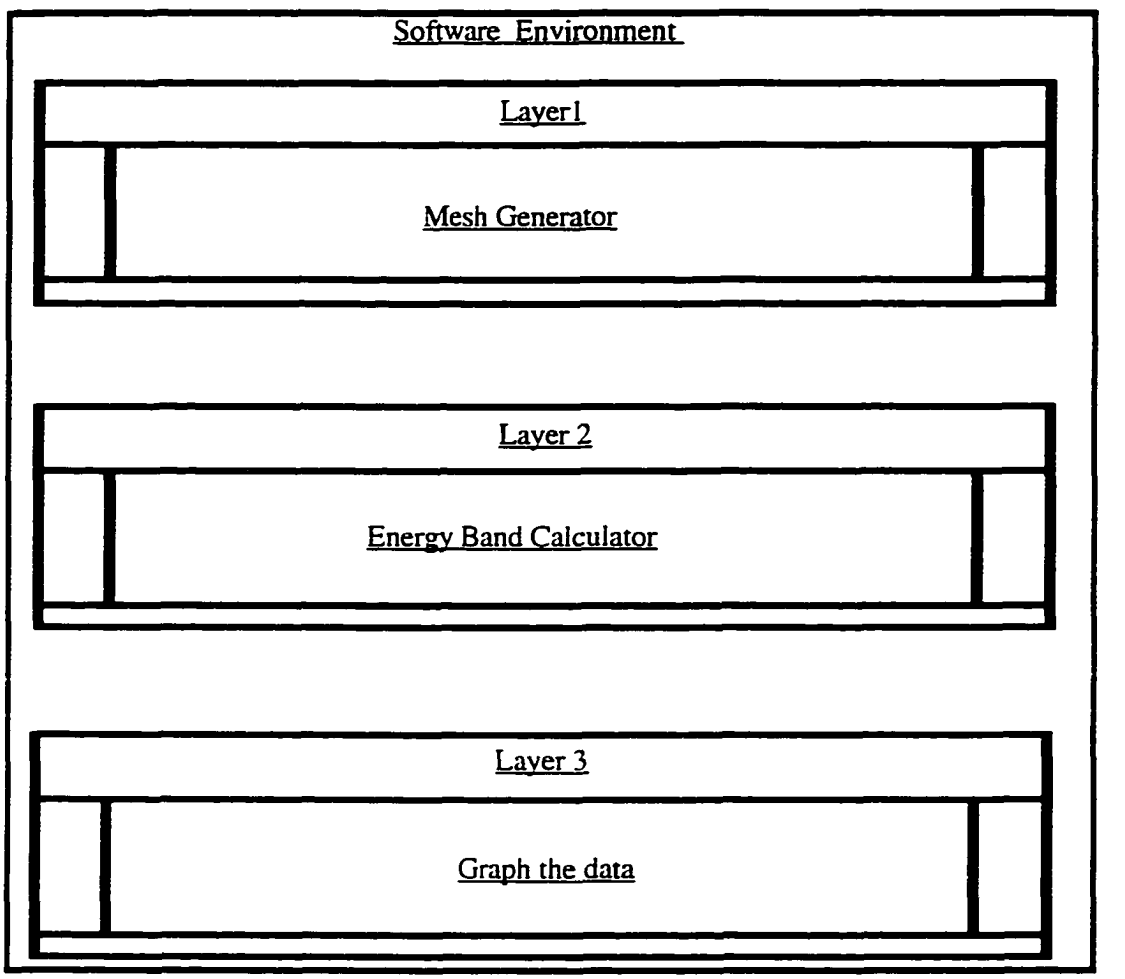


Fig. 6.10. The software modules. Module 1 generates the points and the mesh for the Module 2. Module 2 reads in the mesh generated by module 1 and calculates the electric field. Module 3 graph this calculated points.

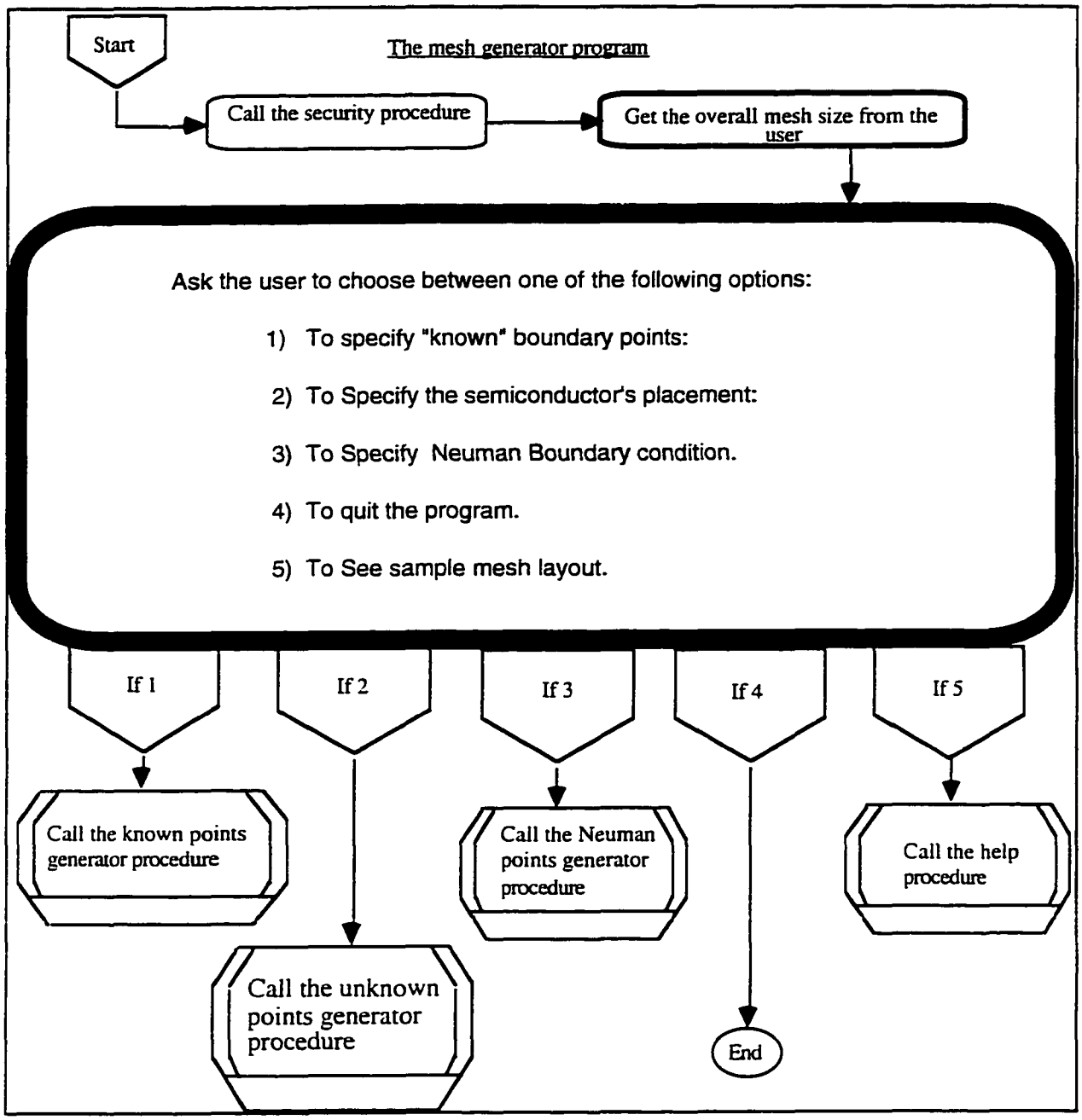


Fig. 6.11. The flow chart for mesh generator program. This program generates 2 files that will be used by the next layer to calculate the electric potential.

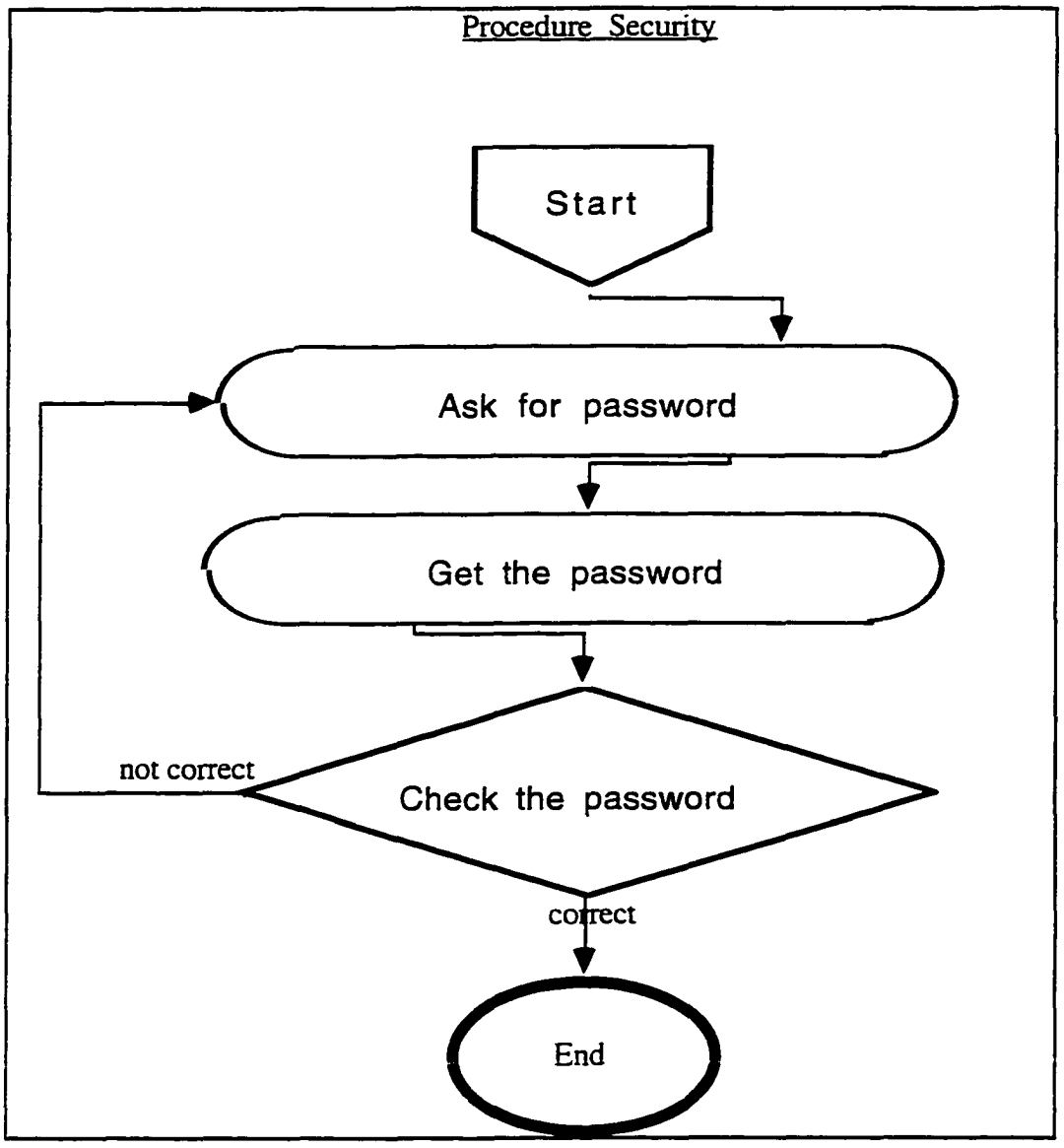


Fig. 6.12. To prevent from unauthorized use of this program a procedure for checking the password using the above algorithm is added to the program.

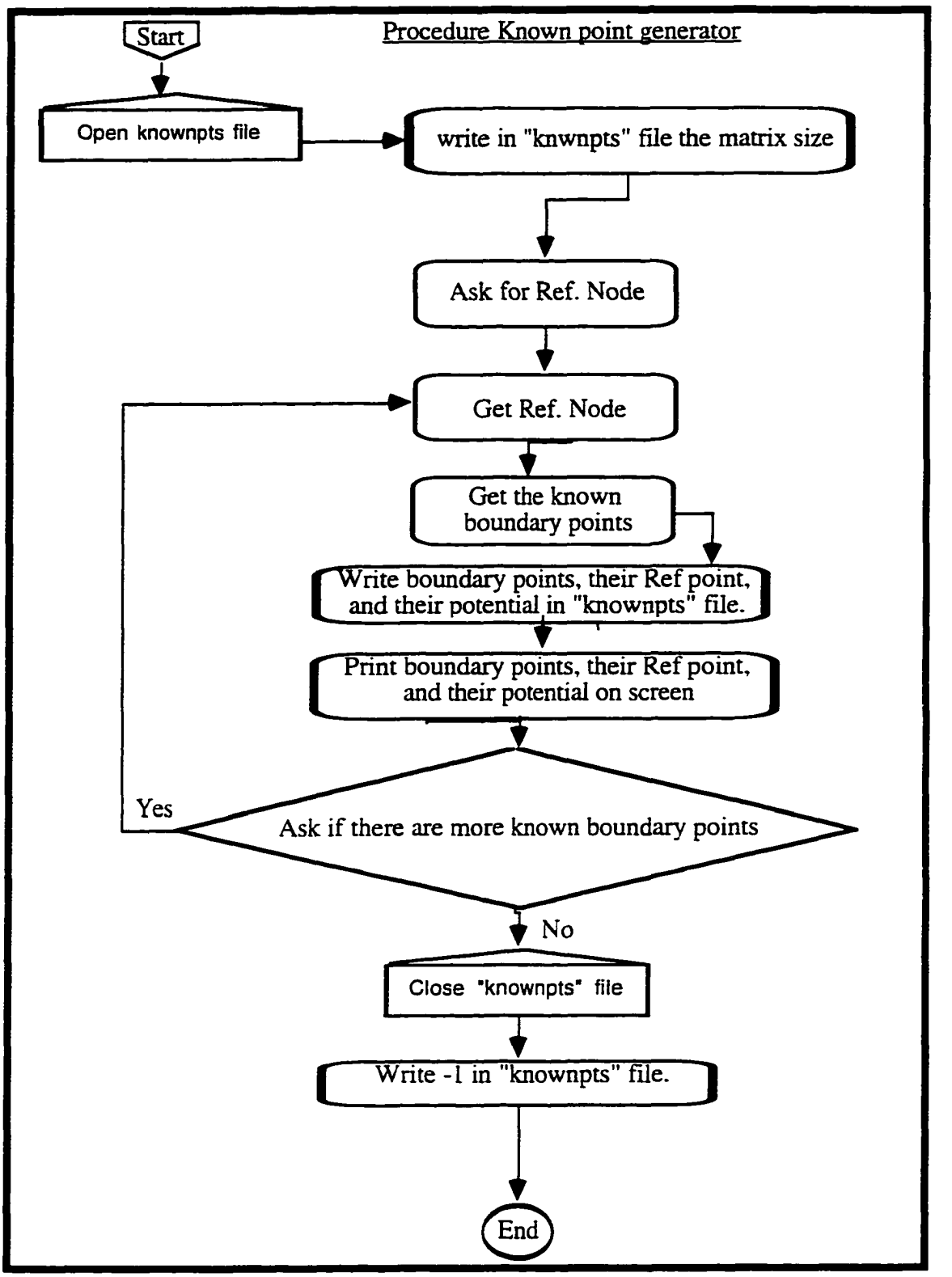


Fig. 6.13. Procedure for generating the known points.

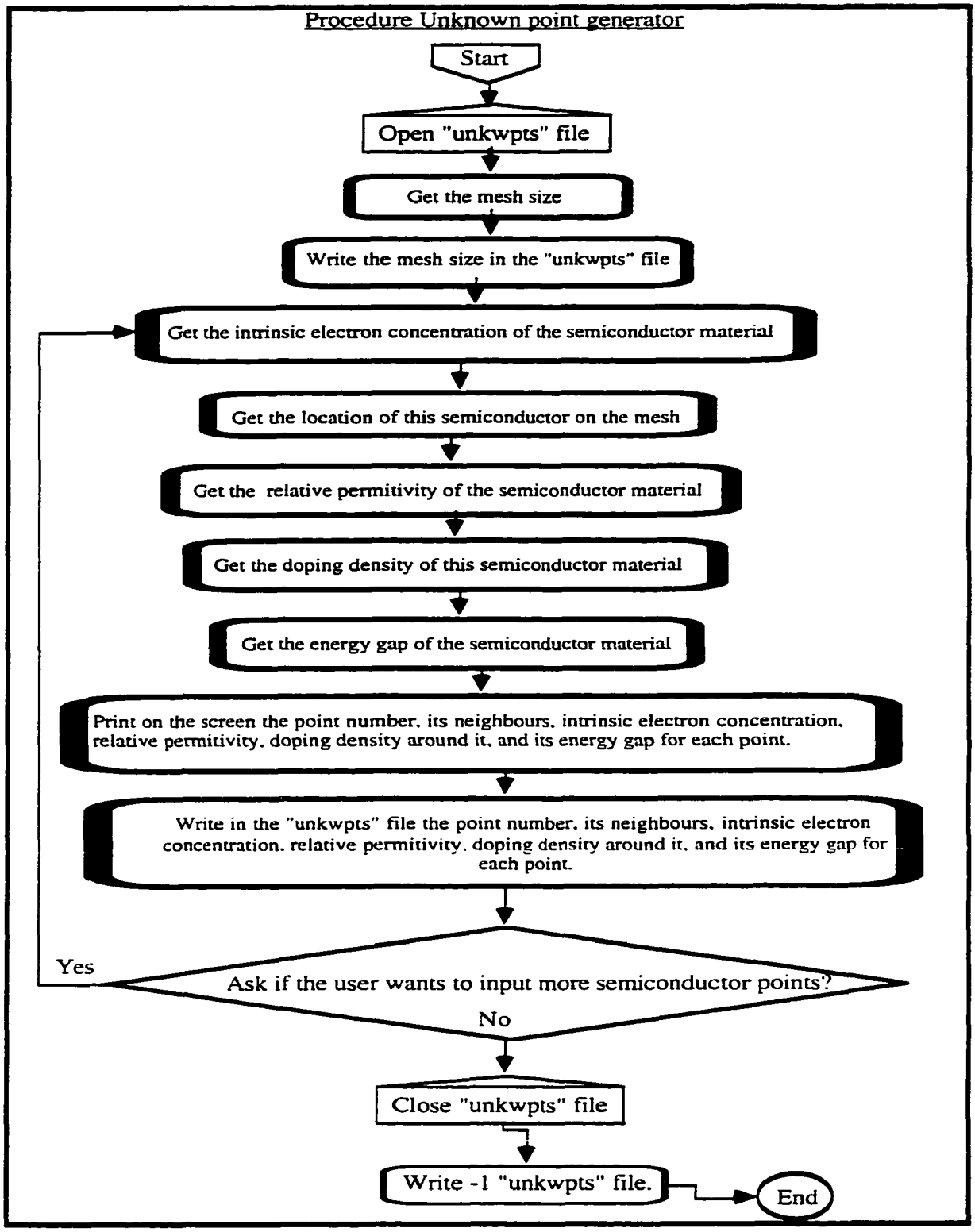


Fig. 6.14. Procedure for generating the unknown points.

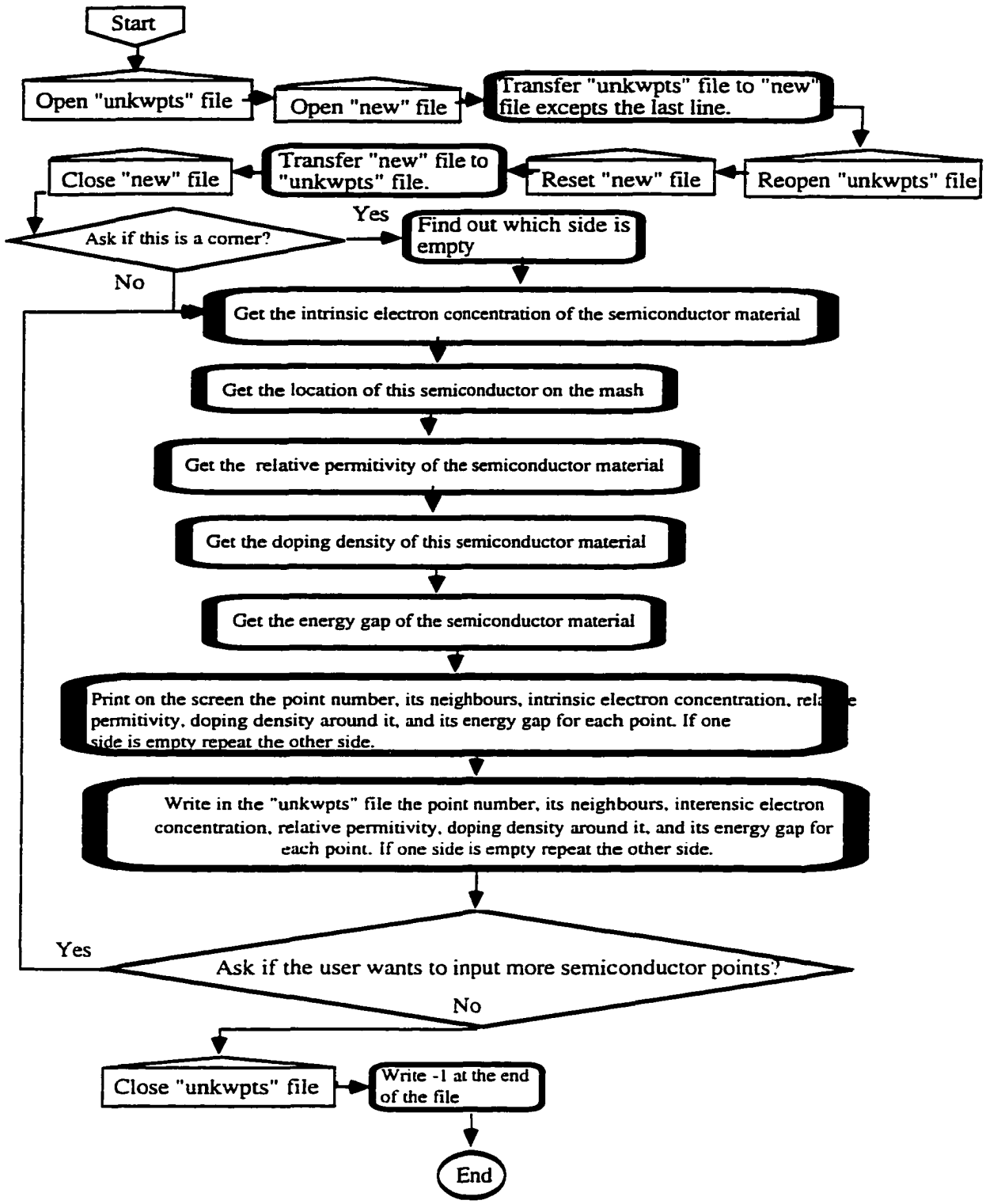


Fig. 6.15. Procedure for generating Neuman points.

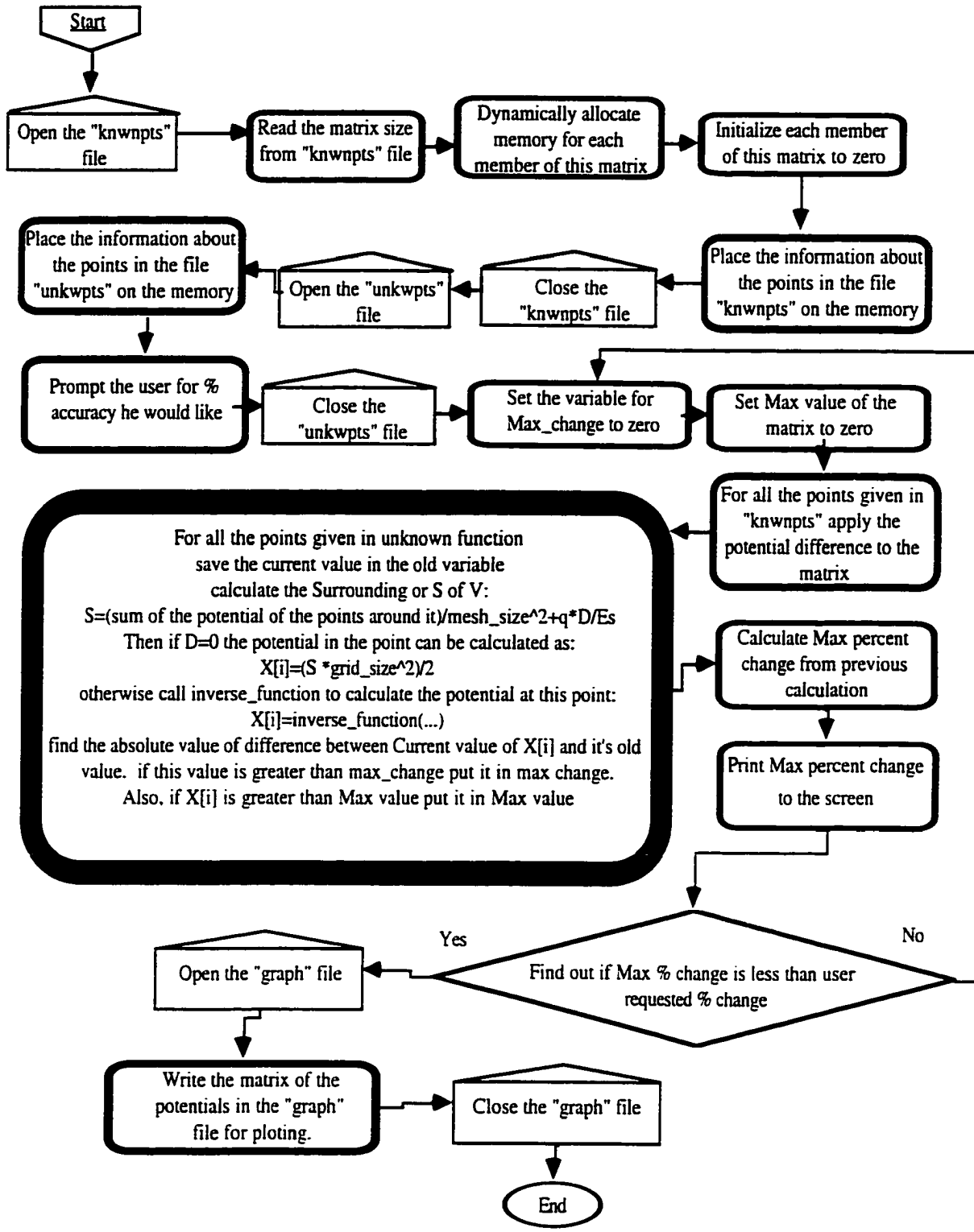


Fig. 6.16. The energy program calculates the potential using FDM analysis.[41-45]

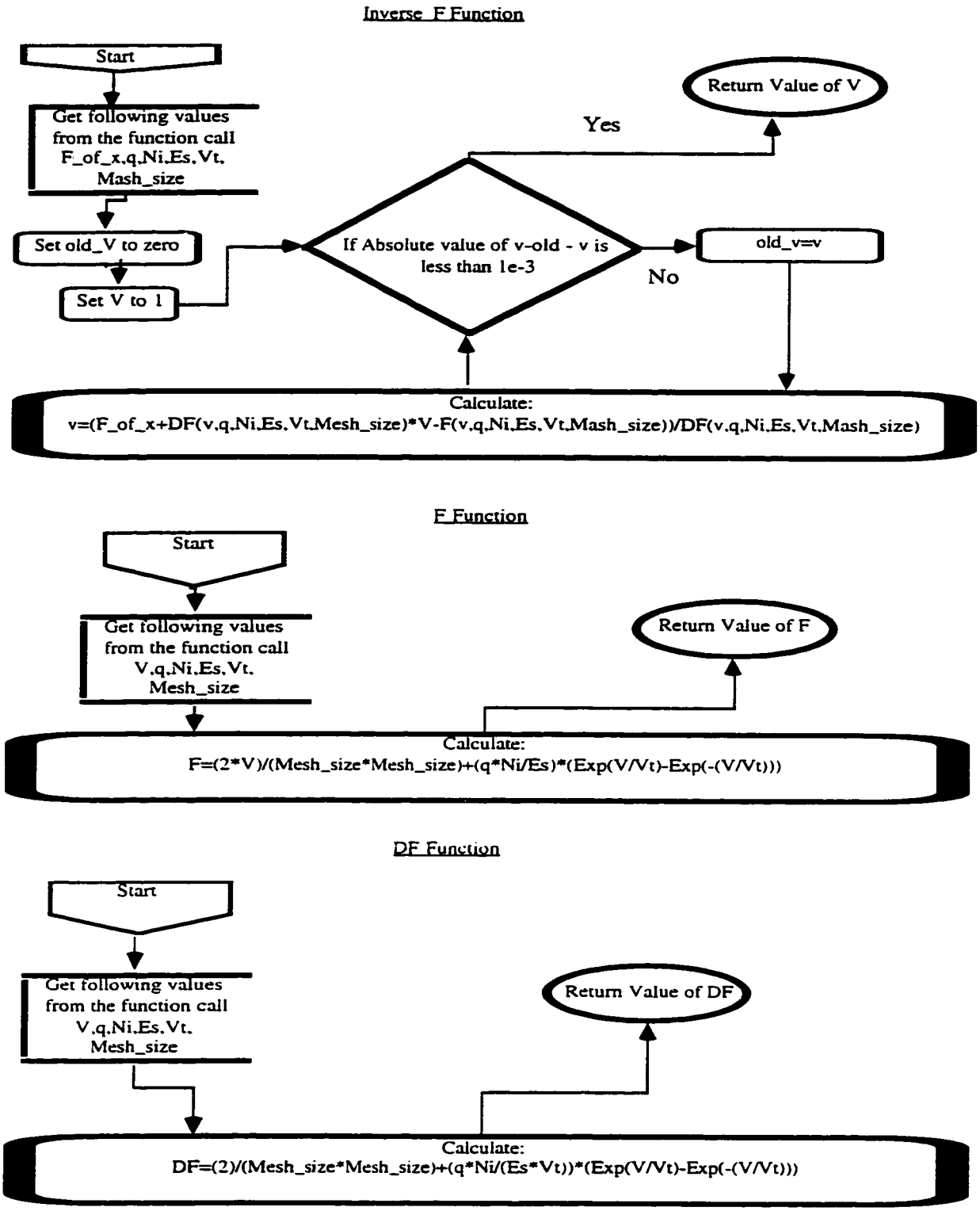


Fig. 6.17. Several functions needed for Energy program to work.

```
program data_generator(input,output);
 var
  row,col,i:integer;
 procedure security;
 var
  id:string;
  match:boolean;
 begin
  repeat
   Write('Enter your designated id? '); readln(id);
   match:= id = 't.p.EE513';
   if(not(match)) then writeln('Wrong.... be my guest. Try again!');
  until(match);
 end;
 procedure known_point_generator(col,Matrix_size:integer);
  var
    knwnpts:text;
    v:real;
    refference_node,end_i,end_j,start_i,start_j,i,j,point_number:integer;
    answer:char;
  begin
    ASSIGN(KNWNPTS,'KNWNPTS');
    Rewrite(KNWNPTS);
    writeln(KNWNPTS,col,'  ',matrix_size);
    write('Enter refference node''s row and col: ');
     readln(i,j);
     refference_node:=j+matrix_size*(i-1);
    WRITELN('************************************************');
    answer:='y';
    Repeat
     WRITELN;
     WRITELN('Get ready to enter known points (Boundery condition)');
     writeln;
     write('Enter starting row to ending row with space in between them:
');
     readln(start_i,end_i);
     write('Enter starting col to ending col with space in between them:
');
     readln(start_j,end_j);
     write('Enter potential (voltage) on these nodes: ');
     readln(v);
     writeln('These  values are generated.');
     writeln;
     writeln('Point Number    refference_node Value of the Voltage');
     writeln('_____________   _______________ ______________________');
     for i:=start_i to end_i do
      for j:=start_j to end_j do
      begin
```

Fig. 6.18. A Pascal program for generating the semiconductor mesh that later will be analyzed by the Energy (Listing 6.5) program.

```
      point_number:=j+matrix_size*(i-1);
      writeln(KNWNPTS,point_number,'   ',refference_node,' ',v);
      writeln('   ',point_number:5,refference_node:15,'           ',v);
      end;
     write('Do you have more Boundery Nodes that have not enter yet? ');
     readln(answer);
    until((answer = 'N') or (answer = 'n'));
    point_number:=-1;
    writeln(KNWNPTS,point_number,'   ',refference_node,' ',v);
    Close(knwnpts);
  end;
 procedure unknown_point_generator(matrix_size:integer);
  Var
    Eg,Ni,Er,v,h:real;
    start_j,end_j,start_i,end_i,i,j,point_number,e,n,w,s:integer;
    UNKWPTS:text;
    answer:char;
  begin
    ASSIGN(UNKWPTS,'UNKWPTS');
    Rewrite(UNKWPTS);
    WRITELN('************************************************');
    WRITELN;
    WRITELN('Get ready to enter the unknown points ');
    writeln;
    write('What is the mash size? ');
    readln(h);
    writeln(UNKWPTS,h);
    answer:='y';
    Repeat
      Write('Enter Ni (interensic electron concentration)[e/Cm3]');
      readln(Ni);
      write('Enter starting row to ending row with space in between them:
');
      readln(start_i,end_i);
      write('Enter starting col to ending col with space in between them:
');
      readln(start_j,end_j);
      write('Enter reletive permitivity of this space [no units]: ');
      readln(Er);
      write('Enter the doping density in this space (+ for acceptor Na)
:');
      readln(v);
      write('Enter Energy gap of your semiconductor (ev):');
      readln(Eg);
      writeln('Point_number      e      w     D         Er      Ni
Eg');

writeln('_____________________________________________________________')
;
      For i:=start_i to end_i do
```

Fig. 6.18. Continued.

```
      for j:=start_j to end_j do
        begin
          point_number:=j+matrix_size*(i-1);
          e:=point_number+1;
          w:=point_number-1;
          writeln(UNKWPTS,Point_number,' ',e,' ',w,' ',Ni,' ',v,' ',Er,'
',Eg);
          write(Point_number:7,'        ',e:5,' ',w:5);
          writeln( '   ',v:6,'  ',Er:6:2,' ', Ni:6,' ',Eg:5:2);
      End;
      write('Do you have more Boundery Nodes that have not enter yet? ');
      readln(answer);
    until((answer = 'N') or (answer = 'n'));
    point_number:=-1;
    writeln(UNKWPTS,Point_number,' ',e,' ',w,' ',Ni,' ',v,Er,' ',Eg);
    close(UNKWPTS);
  end;
 procedure neuman_point_generator(matrix_size:integer);
  Var
    Ni,Er,v,h,Eg:real;
    start_j,end_j,start_i,end_i,i,j,point_number,e,n,w,s:integer;
    ie, en, iw, is :integer;
    new,UNKWPTS:text;
    answer:char;
  begin
    ASSIGN(UNKWPTS,'UNKWPTS');
    Reset(UNKWPTS);
    assign(new,'new');
    rewrite(new);
    readln(UNKWPTS,h);
    writeln(new,h);
    repeat
      readln(UNKWPTS, Point_number,e,w,Ni,v,Er,Eg);
      writeln(new,Point_number,' ',e,' ',w,' ',Ni,' ',v,' ',Er,' ',Eg);
    until(point_number < 0);
    close(new);
    close(UNKWPTS);
    reset(new);
    rewrite(UNKWPTS);
    readln(new,h);
    writeln(UNKWPTS,h);
    readln(new,Point_number,e,w,Ni,v,Er,Eg);
    repeat
      writeln(UNKWPTS,Point_number,' ',e,' ',w,' ',Ni,' ',v,' ',Er,' ',Eg);
      readln(new,Point_number,e,w,Ni,v,Er,Eg);
    until(point_number < 0);
    close(new);
    WRITELN('************************************************');
    WRITELN;
    WRITELN('Get ready to enter the neuman points ');
```

Fig. 6.18. Continued.

```
    writeln;
     answer:='y';
     Repeat
       ie:=0;
       iw:=0;
       en:=0;
       is:=0;
       write('Is this a corner? ');readln(answer);
   case answer of
     'y','Y' : i:=0;
     'n' ,'N' : i:=1;
   end;
    repeat
      i:=i+1;
       write('Which side sides is/are empty e or w (one at a time)? ');
       readln(answer);
       case answer of
       'E','e' : ie:=-2;
       'w','W' : iw:=2;
       's','S' : is:=2*matrix_size;
       'n','N' : en:=-2*matrix_size;
       end;
    until ( i =2);
       Write('Enter Ni (interensic electron concentration)[e/Cm3]');
       readln(Ni);
       write('Enter Energy gap(ev):');
       readln(Eg);
       write('Enter starting row to ending row with space in between them:
');
       readln(start_i,end_i);
       write('Enter starting col to ending col with space in between them:
');
       readln(start_j,end_j);
       write('Enter reletive permitivity of this space ');
       readln(Er);
       write('Enter the doping density in this space (+ for acceptor Na)
:');
       readln(v);
       writeln('Point_number      e      w     D          Er      Ni
Eg');

writeln('_____________________________________________________________
___');
       For i:=start_i to end_i do
        for j:=start_j to end_j do
          begin
            point_number:=j+matrix_size*(i-1);
            e:=point_number+1+ie;
            w:=point_number-1+iw;
            writeln(UNKWPTS,Point_number,' ',e,' ',w,' ',Ni,' ',v,' ',Er,'
',Eg);
```

Fig. 6.18. Continued.

```
          write(Point_number:7,'        ',e:5,'   ',w:5);
          writeln('    ',v:6,'  ',Er:6:2,'  ',Ni:6,' ',Eg);
      End;
      write('Do you have more Boundery Nodes that have not enter yet? ');
      readln(answer);
    until((answer = 'N') or (answer = 'n'));
    point_number:=-1;
    writeln(UNKWPTS,Point_number,' ',e,' ',w,' ',Ni,' ',v,' ',Er,' ',Eg);
    close(UNKWPTS);
  end;
 procedure help;
 begin
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('Note:row or col numbering start from 1.                       ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                              North                           ');
   writeln('                                                              ');
   writeln('                        ┌┬┬┬┬┬┬┬┬┬┐                          ');
   writeln('                        ├┼┼┼┼┼┼┼┼┼┤                        ');
   writeln('           W          ^ ├┼┼┼┼┼┼┼┼┼┤      E                 ');
   writeln('           e          . ├┼┼┼┼┼┼┼┼┼┤      a                 ');
   writeln('           s   r      . ├┼┼┼┼┼┼┼┼┼┤      s                 ');
   writeln('           t   o      . ├┼┼┼┼┼┼┼┼┼┤      t                 ');
   writeln('               w      3 ├┼┼┼┼┼┼┼┼┼┤                        ');
   writeln('                      2 ├┼┼┼┼┼┼┼┼┼┤                        ');
   writeln('                      1 └┴┴┴┴┴┴┴┴┴┘                         ');
   writeln('                        1 2 3... Ø Ø                          ');
   writeln('                            col                               ');
   writeln('                                 South                        ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('                                                              ');
   writeln('Make sure to incloud refference point in the mash
configureation ');
   writeln('                                                              ');
```

Fig. 6.18. Continued.

```
    writeln('                                                          ');
    writeln(' Press any key to continue.                               ');
    readln;
  end;
  begin
    writeln(' ********************************************************');
    writeln;
    writeln;
    writeln('              Well Come To Babak''s Preprocessor');
    writeln('                           Program ');
    writeln;
    writeln;
    writeln;
    security;
    writeln('How many row & col do you have in your matrix? ');
    writeln('Put space between row and col when you entering them');
    readln(row, col);
  repeat
    for i:=1 to 60 do writeln;
    writeln(' ********************************************************');
    writeln;
    writeln;
    writeln('              Well Come To Babak''s Preprocessor');
    writeln('                           Program');
    writeln;
    writeln;
    writeln;
    writeln('   Please choose one of the following:                ');
    writeln('                                                        ');
    writeln('         1) To spacify the "known" points.              ');
    writeln('                                                        ');
    writeln('         2) To the Mash''s configuration "known points". ');
    writeln('                                                        ');
    writeln('         3) To spacify the Neuman Boundery condition.   ');
    writeln('                                                        ');
    writeln('         4) To quit the Program.                        ');
    writeln('                                                        ');
    writeln('         5) To see the sample mash layout.              ');
    writeln('                                                        ');
    writeln('                                                        ');
    write('Choose between 1-5 ?');
    readln(i);
      case i of
        1 : known_point_generator(row,col);
        2 : unknown_point_generator(col);
        3 : neuman_point_generator(col);
        4 : writeln(' Good Bye!');
        5 : help;
      end;
    until(i = 4);
  end.
```

Fig. 6.18. Continued.

```
{  BaEsma Allaha Rahmana Rahim }
program Finite_difference_methode_for_semiconductors(input,output);
  type
    matrix_pointer=^matrix;
    matrix=record
         V:real;
           Eg:real;
         next_matrix_pointer:matrix_pointer;
         end;
    unknown_matrix_pointer=^unknown_config;
    unknown_config=record
                point_no:matrix_pointer;
                e:matrix_pointer;
                w:matrix_pointer;
                D:real;
                Ni:real;
                Es:real;
                next_unknown_pointer:unknown_matrix_pointer;
                end;
    known_matrix_pointer=^known_config;
    known_config=record
              high:matrix_pointer;
              low:matrix_pointer;
              dif:real;
              next_known_pointer:known_matrix_pointer;
              end;
    set_no_1='e'..'w';
  Const
    Eo=8.85e-14;    {farads/cm}
    q=1.6e-19;       {columb}
    Vt=0.0259;       {volts  KT/q}
   {  ************************************************************************
       before runing the program make sure to change matrix size to correct
value
       the correct vale is the total number of points you have, also
generate two input
       files called KNWNPTS and UNKWPTS and end these files with negative
       value for the point number in the UNKWPTS give the mash size first
thing

       sample for known points file    sample for unknown points file
       ____________________________    ______________________________
     # of rows     # of col
   high pt#,low pt#,pot dif(V)                mashsize [should be real]
              :                  pointnumber,e,w,Ni,Doping,Density,Er,Eg
              :                                  :
              :                                  :
              :                                  :
        -something                                    -something
```

Fig. 6.19. Following Pascal program reads the files generated by Prepro program (Listing 6.4) and calculates the potentioals (ie. Energies in verious points of the semiconductor)

```
**********************************************************************}
Var
    UNKWPTS,KNWNPTS,GRAPH:TEXT;
    Sranding,Abs_Change,Abs_x,grid_Size:real;
    Ni:real;    {electron/Cm3 interensic density of electrons}
    Es:real;        {total dielectric constant.}
    D:real; { Doping density  + for acceptor and - for doner }

Old,V,Max_x,Max_Change,Change,Acceleration,percent_prs_req,Error,L,sum1,sum
2:real;
    Er:real;       { realative dielectric constant at each point}
    i,n,s,w,e,j,counter:integer;
    high,low,row,col,matrix_size:integer;
    Eg,Ef,Ei,Ev,Ec,dif:real;
    X:array [set_no_1] of real;
    start_known_pointer,current_known_pointer:known_matrix_pointer;
    start_unknown_pointer,current_unknown_pointer:unknown_matrix_pointer;
    start_matrix_pointer,current_matrix_pointer:matrix_pointer;
            {                ************************
                      Here is the founction to calculate the inverse of
F(X)
                              ************************             }

  Function Inverse_F(F_of_x,q,Ni,Es,Vt,Mash_size:Real):Real;
     var
     old_v:real;
     Function F(V,q,Ni,Es,Vt,Mash_size:Real):Real;
       begin
       F:=(2*V)/(Mash_size*Mash_size)+(q*Ni/Es)*(Exp(V/Vt)-Exp(-(V/Vt)));
       end;
     Function DF(V,q,Ni,Es,Vt,Mash_size:Real):Real;
       begin
       DF:=(2)/(Mash_size*Mash_size)+(q*Ni/(Es*Vt))*(Exp(V/Vt)+Exp(-
(V/Vt)));
       end;
     begin
       OLD_V:=0;
       V:=1;
       While(Abs( old_v-v) > 1e-3) do
       begin
         old_v:=v;
         V:=(F_of_x + DF(V,q,Ni,Es,Vt,Mash_size)*V -
F(V,q,Ni,Es,Vt,Mash_size)
                                          )/ DF(V,q,Ni,Es,Vt,Mash_size);
       end;
       Inverse_F:=V;
     End;
            {              ************************
                     Main body of program starts here
                        ************************      }
```

Fig. 6.19. Continued.

```
Begin
   assign(knwnpts,'knwnpts');
   reset(knwnpts);
   readln(knwnpts,row,col);
   matrix_size:=row*col;
   new(start_matrix_pointer);
   current_matrix_pointer:=start_matrix_pointer;
               {
                     ************************
               Forming the matrix and initating it to zero
                     ************************
                                          }
   for i:=2 to matrix_size do
     begin
     current_matrix_pointer^.v:=0;
     new(current_matrix_pointer^.next_matrix_pointer);
     current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
     end;
               {
                      *****************
                     matrix is formed now
                      *****************
                      }
   current_matrix_pointer^.next_matrix_pointer:=nil;

         { We are reading all the known or Dirichlet points}

   new(start_known_pointer);
   current_known_pointer:=start_known_pointer;
   readln(knwnpts,high,low,dif);
   while(high>0) do
     begin
     current_matrix_pointer:=start_matrix_pointer;
     For i:=2 to high do
       begin

current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
       end;
     current_known_pointer^.high:=current_matrix_pointer;
     current_matrix_pointer:=start_matrix_pointer;
     For i:=2 to low do
       begin

current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
       end;
     current_known_pointer^.low:=current_matrix_pointer;
     current_known_pointer^.dif:=dif;
     readln(knwnpts,high,low,dif);
     if (high>0) then
       begin
         new(current_known_pointer^.next_known_pointer);
```

Fig. 6.19. Continued.

```
          current_known_pointer:=current_known_pointer^.next_known_pointer;
        end;
      end;
    current_known_pointer^.next_known_pointer:=nil;
    current_matrix_pointer:=start_matrix_pointer;
    close(knwnpts);

              { We rad all the known or Dirichlet points}

              {        readig the unknown points       }
    new(start_unknown_pointer);
    current_unknown_pointer:=start_unknown_pointer;
    assign(UNKWPTS,'unkwpts');
    reset(unkwpts);
    readln(unkwpts,grid_size);
    readln(unkwpts,i,e,w,Ni,D,Er,Eg);
       current_unknown_pointer^.D:=D;
       current_unknown_pointer^.Ni:=Ni;
       current_unknown_pointer^.Es:=Er*Eo;
       high:=i;
       current_matrix_pointer:=start_matrix_pointer;
       For j:=2 to high do
        begin

current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
        end;
      current_unknown_pointer^.point_no:=current_matrix_pointer;
        current_matrix_pointer^.Eg:=Eg;
       high:=e;
       current_matrix_pointer:=start_matrix_pointer;
       For j:=2 to high do
        begin

current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
        end;
      current_unknown_pointer^.e:=current_matrix_pointer;
       high:=w;
       current_matrix_pointer:=start_matrix_pointer;
       For j:=2 to high do
        begin

current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
        end;
      current_unknown_pointer^.w:=current_matrix_pointer;
    readln(unkwpts,i,e,w,Ni,D,Er,Eg);
    while (i > 0) do
      begin
       new(current_unknown_pointer^.next_unknown_pointer);

current_unknown_pointer:=current_unknown_pointer^.next_unknown_pointer;
       current_unknown_pointer^.D:=D;
```

Fig. 6.19. Continued.

```
        current_unknown_pointer^.Ni:=Ni;
        current_unknown_pointer^.Es:=Er*Eo;
        high:=i;
        current_matrix_pointer:=start_matrix_pointer;
        For j:=2 to high do
         begin
current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
         end;
       current_unknown_pointer^.point_no:=current_matrix_pointer;
         current_matrix_pointer^.Eg:=Eg;
        high:=e;
        current_matrix_pointer:=start_matrix_pointer;
        For j:=2 to high do
         begin
current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
         end;
       current_unknown_pointer^.e:=current_matrix_pointer;
        high:=w;
        current_matrix_pointer:=start_matrix_pointer;
        For j:=2 to high do
         begin
current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
         end;
       current_unknown_pointer^.w:=current_matrix_pointer;
         readln(unkwpts,i,e,w,Ni,D,Er,Eg);
       end;
       current_unknown_pointer^.next_unknown_pointer:=nil;
       close(unkwpts);
                    {
                   ********************
                   End of file reading
                   ********************
                   }
     write('Enter accuracy:');readln(percent_prs_req);
     Acceleration:=1;
     Repeat
       Max_X:=0;
       Max_Change:=0;
       current_known_pointer:=start_known_pointer;
       while (current_known_pointer <> nil ) do
       begin
         current_known_pointer^.high^.v:=current_known_pointer^.low^.v +
                     current_known_pointer^.dif;
         current_known_pointer:=current_known_pointer^.next_known_pointer;
       end;
       current_unknown_pointer:=start_unknown_pointer;
       while (current_unknown_pointer <> nil ) do
      begin
       X['i']:=current_unknown_pointer^.point_no^.v;
       X['n']:=0;
       X['e']:=current_unknown_pointer^.e^.v;
       X['w']:=current_unknown_pointer^.w^.v;
       X['s']:=0;
```

Fig. 6.19. Continued.

```
        Es:=current_unknown_pointer^.Es;
        D:=current_unknown_pointer^.D;
        Ni:=current_unknown_pointer^.Ni;
        old:=x['i'];
        Sranding:=(X['e']+X['n']+X['w']+X['s'])/(grid_Size*grid_Size)+
q*D/Es;
          IF(D=0) THEN
            X['i']:=SRANDING*GRID_SIZE*GRID_SIZE/2
          ELSE
            X['i']:=Inverse_F(Sranding,q,Ni,Es,Vt,grid_Size);
        Change:=x['i']-Old;
        X['i']:=Old+Acceleration*change;
        Abs_Change:=Abs(Change);
        Abs_x:=Abs(X['i']);
        If Abs_Change >Max_Change then Max_Change:=Abs_Change;
        If Abs_x >Max_X then Max_X:=Abs_x;
        current_unknown_pointer^.point_no^.v:=X['i'];

current_unknown_pointer:=current_unknown_pointer^.next_unknown_pointer;
       end;
        Error:=100*Max_change/Max_x;writeln(error);
     Until(error< percent_prs_req);
                          {         *****************
        Now our matrix is evaluated so we can start pripareing the data for
                                 ploting.
                                 ******************   }
     current_known_pointer:=start_known_pointer;
       while (current_known_pointer <> nil ) do
       begin
         current_known_pointer^.high^.v:=current_known_pointer^.low^.v +
                      current_known_pointer^.dif;
         current_known_pointer:=current_known_pointer^.next_known_pointer;
       end;
     assign(graph,'graph');
     REWRITE (GRAPH);
      writeln(graph,'D  r0 y1 g2 r0');
      WRITELN(GRAPH,'   ',matrix_size,'  4 ');
      current_matrix_pointer:=start_matrix_pointer;
      Ef:=4.5;
      d:=0.0;
      repeat
        d:=d+0.1;
        Eg:=current_matrix_pointer^.Eg;
        Ei:=Ef-current_matrix_pointer^.v;
        Ev:=Ei-Eg/2;
        Ec:=Ei+Eg/2;
        writeln(graph,d:5:2,' ',Ec,' ',Ei,' ',Ef,' ',Ev);
current_matrix_pointer:=current_matrix_pointer^.next_matrix_pointer;
      Until( current_matrix_pointer=nil);
     Close(GRAPH);
  End.
```

Fig. 6.19. Continued.

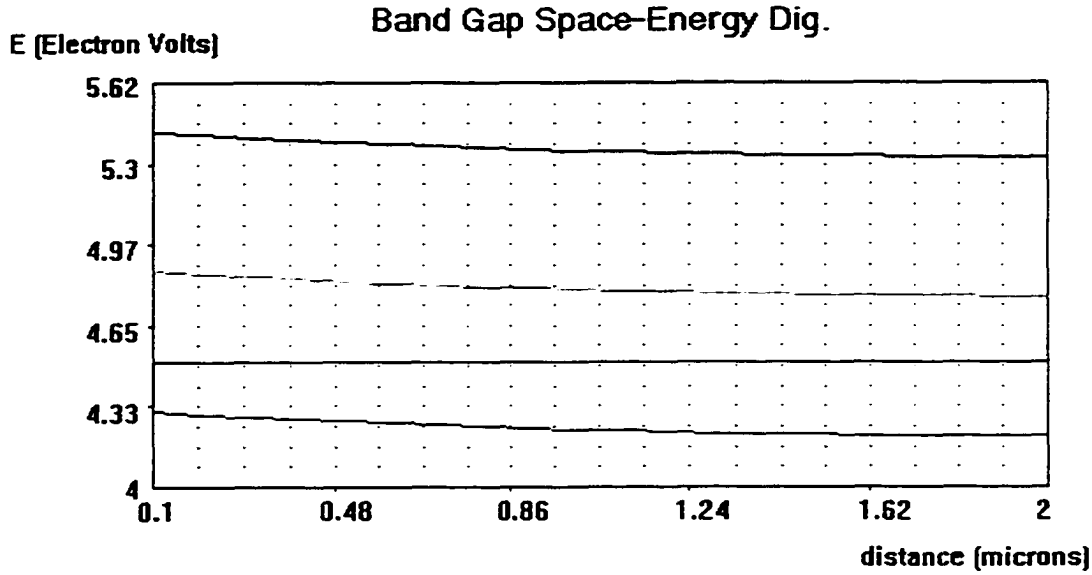


Fig. 6.20. An ohmic contact using on P-type semiconductor verified by this simulation program.

7. EXPERIMENTAL VERIFICATION OF INTER-LAYER SHIELD

To verify the theoretical results obtained in previous sections, it was decided to devise an experiment and test the effectiveness of our shield. To accomplished this task, given the means available to me, I decided to use double sided polished silicon wafers for the base material.

Two sets of double sided polished silicon wafers of the same thickness and similar characteristics were selected. The wafers used in this experiment were all n-type with bulk resistivity of 4 to 8 Ohm-cm. The structures in Fig. 7.1 A and 7.1 B were fabricated on sets A and B respectively. It can be observed from Fig. 7.1 A and 7.1 B that these structures are very similar. Both sets of silicon wafers are sandwiched between oxide layers on each side. Note that in set B there is a thin 2 μm n^+ diffused region just before the oxide in one side of the wafers. This n^+ region is our shield region. Finally, all the wafers were metalized on both side and pattern of the Figure 7.2 was etched on both side. Note that the parallel lines at the back of the wafers were aligned with the corresponding parallel lines in front of the wafer using infrared photolithography.

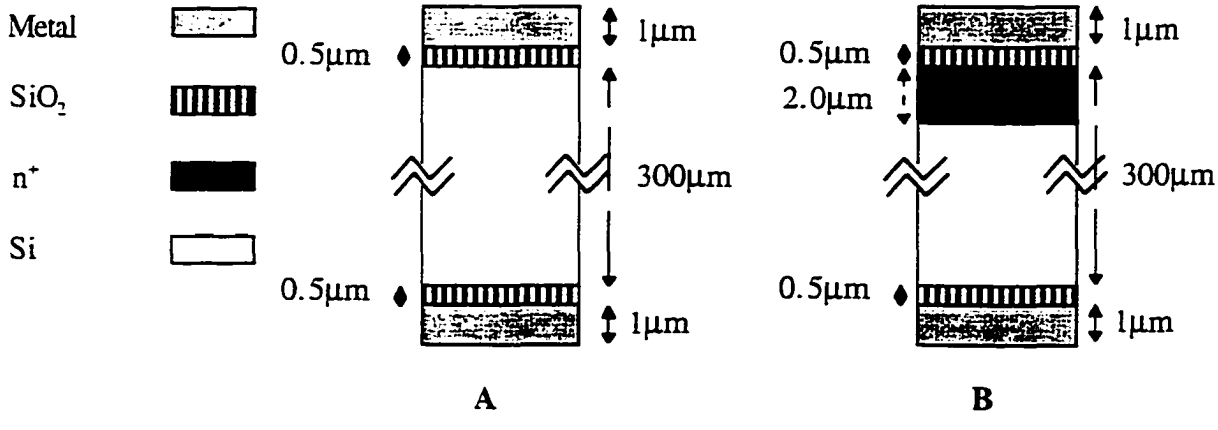


Fig. 7.1. Structure designed to test the shield structure.

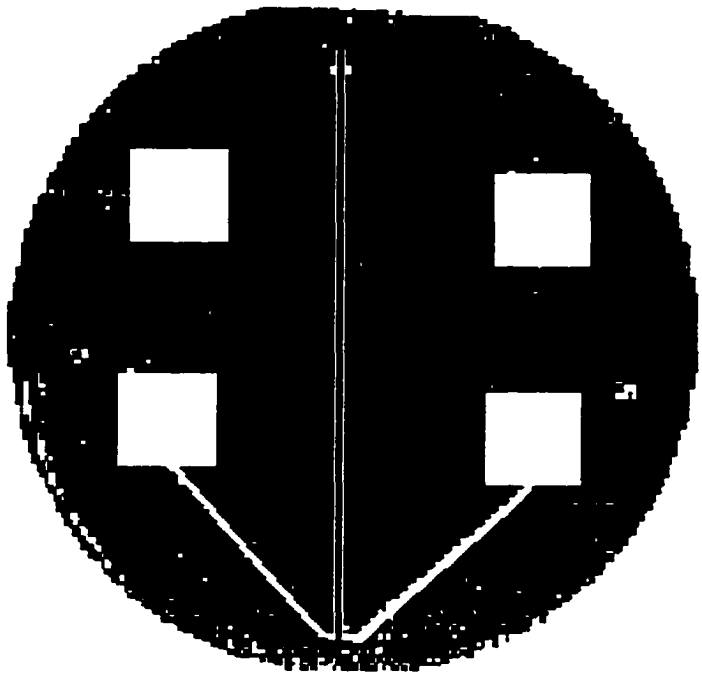


Fig. 7.2. Test pattern etched on both sides of the wafer to test the performance of the shield.

To test the effectiveness of the shielding mechanism, parallel lines of each side of the wafer is connected to ports of a network analyzer. Then the scattering parameter S_{12} is measured. Note that S_{12} is defined as follows with respect to figure 7.3:

$$S_{ij} = \frac{\frac{V_j^-}{\sqrt{Z_{oj}}}}{\frac{V_i^+}{\sqrt{Z_{0i}}}} \qquad \text{Eq. 7.1}$$

Therefore:

$$\left|\frac{P_{out}}{P_{in}}\right| = \frac{\frac{|V_j^-|^2}{|Z_{oj}|}}{\frac{|V_i^+|^2}{|Z_{oi}|}} = |S_{ij}|^2 \qquad \text{Eq. 7.2}$$

It was expected that this measurement be consistent with the results obtained in Chapter 2. However, due to several facts including the frequency dependence of the connecting network to the network analyzer, frequency dependence of the test structure itself, radiation pattern characteristics of the test structure, and the fact that carrier electrons inside the shield have inertia and they impose a reactive term on bulk resistivity of the wafer. These influences create some deviation from expected results for purely resistive material. The reactive term of resistivity will be further discussed when we review the results later in this chapter.

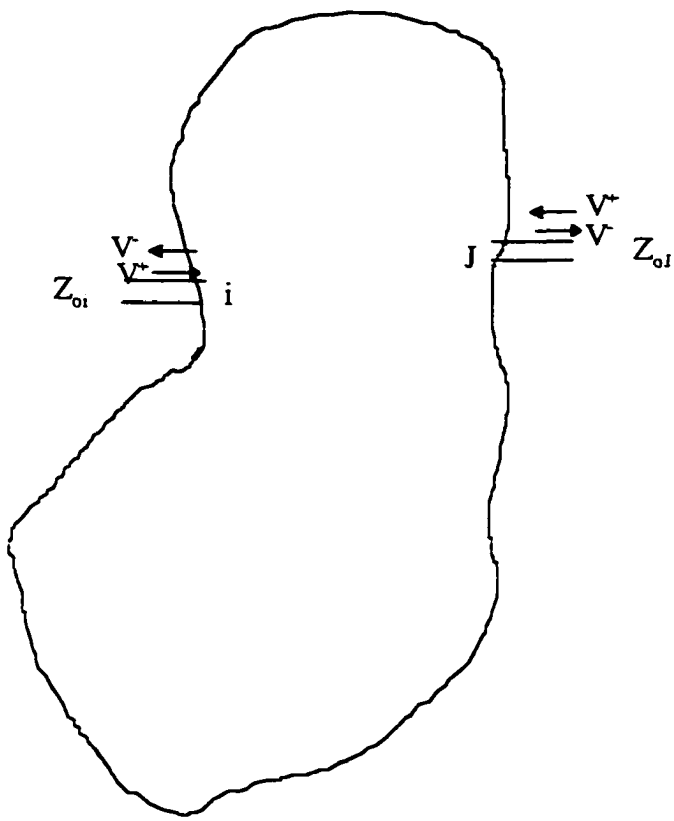


Fig. 7.3. Scattering parameter for n port network

7.1. SUPREM III Simulation of the experiment

It was decided to simulate the process designed to build experimental structures presented in Fig. 7.1 before fabricating it. Process simulation for structures 7.1.A and 7.1.B are presented at the end of this section in Fig. 7.5 and 7.6 respectively.

As it can be seen in these listings to fabricate structure shown in Fig. 7.1.A, first we load the wafers in to diffusion tube at 800° C temperature. Then we ramp up the temperature of these wafers to 1100° C under a flow of nitrogen gas. After the wafers reach this temperature, water vapor and oxygen is forced into the tube were the wafers are located. They remain under this condition for 36 minutes. After this stage is complete, the water vapor and oxygen are stopped and the tube is switched to nitrogen source and the temperature is ramped down to 800 °C. Next, we metalize both sides of the wafers using spattering techniques with silicon doped Al. We cover both sides of the wafers with photo-resist and expose only one side of the wafers. This allows us to etch the pattern in one side of the wafers without effecting the other side. At this stage a alignment window is etched from the other side of the wafer. Then the pattern in the other side of the wafers are aligned using infrared photolithography and alignment windows. At this stage the patterned metal side of the wafers are masked with photo-resist to protect them from etching solution. Finally the pattern generated by infrared photo lithography is etch from the other side of the wafers.

A brief description of the process to fabricate the structure in Fig. 7.1.B is as follows: An oxide layer of 0.5 μm is grown on both sides of the wafers using wet oxide process similar to process used above. Then photo-resist is used to mask on side of the wafer. Then the wafer is put inside oxide etching mixture to remove the oxide from the other side of the wafer. The photo-resist is removed using acetone and other solutions. Next a solid source is then to create a highly doped phosphorous region on the surface of the wafer. Then, an oxidation

process similar to one used to fabricate structure in Fig. 7.1.A is used to oxidize the wafers. Fig. 7.4 presents SUPREM's plot for the impurity distribution close to the surface of the silicon in structure 7.1.B. We use a method similar to the one used for metalizaion of the structure 7.1.A to metalize both sides of these wafers.

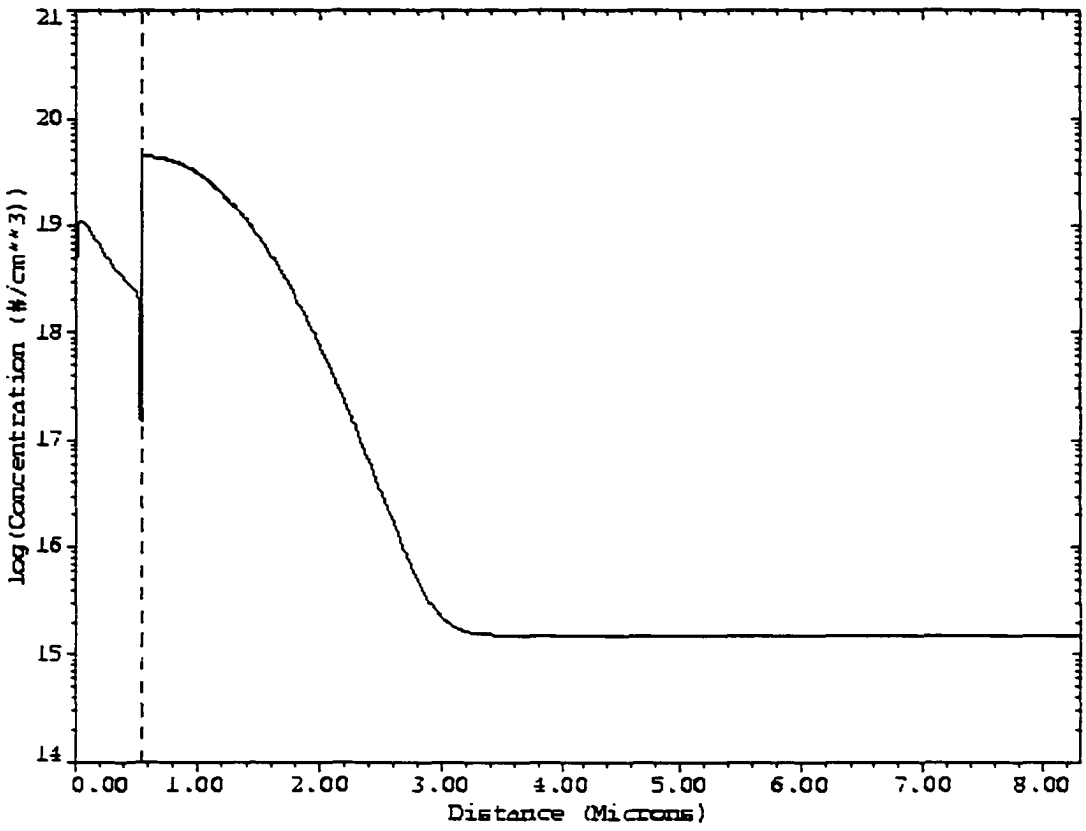


Fig. 7.4. Concentration of n-impurities close to the surface of the structure 7.1.B

```
*************************************************************
***                      SUPREM-3                         ***
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***        Technology Modeling Associates, Inc.           ***
***                 All Rights Reserved                   ***
***                                                       ***
***          Licensed to Iowa State University            ***
***                 Serial # 0155401845                   ***
*************************************************************

                        6-Aug-96 12:33:25

     Statements input from file shield


    1... Title   Shield using the wafer without doping-Cross AA
    2... $Let us start with a <100> silicon substrate with initial
    3... INITIALIZE        SILICON<100> Phosphors=1.5e15
     ... +       THICKNESS=8.0   DX=0.01
    4... SOLUBILITY       BORON SILICON TEMPERATURE
     ... +       TABLE=(700, 800, 900, 1000, 1100, 1200)
    5... SOLUBILITY       BORON SILICON SOLUBILITY
     ... +       TABLE=(9E19, 28E19, 30E19, 34E19, 37E19, 40E19)
    6... IMPURITY         BORON SILICON DIP.0=3.5E9
    7... SEGREGATION      BORON SILICON /AMBIENT TRANS.0=5.5 TRANS.E=1.0
    8... SEGREGATION      BORON SILICON /OXIDE SEG.0=104 SEG.E=0.66
    9... COMMENT OPTIONAL ENHANCEMENT DURING SOAK ONLY
   10... IMPURITY         BORON SILICON TED.0=1E-3 TED.E=-0.8 TED.TAU=10
TED.CONC=1E20
   11... IMPURITY         PHOSPHORS SILICON NE.0=5.0E21 CTN.F=2.85 DIM.0=14E9
     ... +       DIMM.0=4.5E11
   12... SEGREGATION      PHOSPHORS SILICON /AMBIENT TRANS.0=9.5 TRANS.E=0.7
   13... SOLUBILITY       PHOSPHORS SILICON Temperature
     ... +       TABLE=(700, 800, 900, 1000, 1050, 1100)
   14... SOLUBILITY       PHOSPHORS SILICON SOLUBILITY
     ... +       TABLE=(12E19, 42E19, 55E19, 10E19, 12E19, 13E20)
   15... Comment Start with the bare wafer
   16... COMMENT GROW OXIDE
   17... Diffusion        Temperature=800 Time=19 T.RATE=16 NITROGEN
   18... Diffusion        Temperature=1100 Time=36 WETO2
   19... Diffusion        Temperature=1100 Time=70 T.RATE=-4.1 NITROGEN
   20... PRINT   LAYER
   21... etch oxide
   22... COMMENT BEGIN N DIFFUSION
   23... COMMENT PREDEPOSITION
   24... COMMENT SOURCE
   25... DIFFUSION       Temperature=900 TIME=20 ss.PHOSP UD.PHOSP NITROGEN
   26... PRINT LAYER
```

Fig. 7.5. Suprem simulation of fabrication process for structures shown in Fig. 7.1.A.

```
 27... PRINT ELECTRICAL
 28... PLOT    ACTIVE PHOSPHORS COLOR=1 pause
 29... PRINT LAYER
 30... PRINT ELECTRICAL
 31... STOP
```

```
 Input line #   3
 Coefficient data group read
 File: \tma\s3_9002\library\s3cof0
 Date:  8-Jul-96 13:34:45
 Documentation from data file:

 SUPREM-3 Revision 9002 coefficient initialization

1
 Sheild using the wafer without doping-Cross AA
 GROW OXIDE

 Material layer information
 Input line #  20


 layer  material      thickness    dx       xdx  top bottom  orientation
  no.                    (um)     (um)     (um) node  node  or grain size
   2    oxide             .4796   .0100     .00  198   220
   1    silicon          7.7890   .0100     .00  221  1000       <100>

                  Integrated Dopant (#/cm**2)
 layer              Net                          Sum
  no.      active       chemical       active       chemical
   2     5.2427E+09   5.2427E+09   5.2427E+09   5.2427E+09
   1     1.1867E+12   1.1867E+12   1.1867E+12   1.1867E+12
  sum    1.1920E+12   1.1920E+12   1.1920E+12   1.1920E+12

                  Integrated Dopant (#/cm**2)
 layer           phosphorus
  no.      active       chemical
   2     5.2427E+09   5.2427E+09
   1     1.1867E+12   1.1867E+12
  sum    1.1920E+12   1.1920E+12
```

Fig. 7.5. Continued.

```
                Boundary Locations and Integrated Dopant
                Concentrations for Each Diffused Region
 layer   region  type      top       bottom        net           sum
  no.      no.             depth      depth     active Qd    chemical Qd
                           (um)       (um)      (#/cm**2)     (#/cm**2)
   2        1       n      .0000      .4796    5.2427E+09    5.2427E+09
   1        1       n     -.0001     7.7890    1.1867E+12    1.1867E+12
1
 Sheild using the wafer without doping-Cross AA
 SOURCE

 Material layer information
 Input line #  26


 layer  material      thickness    dx       xdx  top bottom  orientation
  no.                   (um)     (um)     (um) node  node  or grain size
   1    silicon         7.7890   .0100     .00  221  1000       <100>

                  Integrated Dopant (#/cm**2)
 layer              Net                          Sum
  no.      active       chemical       active       chemical
   1     3.2652E+15   3.7206E+15   3.2652E+15   3.7206E+15
  sum    3.2652E+15   3.7206E+15   3.2652E+15   3.7206E+15

                  Integrated Dopant (#/cm**2)
 layer           phosphorus
  no.      active       chemical
   1     3.2652E+15   3.7206E+15
  sum    3.2652E+15   3.7206E+15

                Boundary Locations and Integrated Dopant
                Concentrations for Each Diffused Region
 layer   region  type      top       bottom        net           sum
  no.      no.             depth      depth     active Qd    chemical Qd
                           (um)       (um)      (#/cm**2)     (#/cm**2)
   1        1       n     -.0001     7.7890    3.2678E+15    3.7240E+15
1
 Sheild using the wafer without doping-Cross AA
 SOURCE

 Electrical information
 Input line #  27


 Bias step   1


 layer region type  Conductor Bias   Electron Bias    Hole Bias
  no.    no.            (volts)         (volts)        (volts)
   1      1     n                    0.0000E+00     0.0000E+00
```

Fig. 7.5. Continued.

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (#/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	1	n	3.266E+15	3.2422E-02	3.0843E+01	3.7306E+02	2.6806E-03

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (#/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	1	n	0.000E+00	0.0000E+00		0.0000E+00	1

Sheild using the wafer without doping-Cross AA
SOURCE

Material layer information
Input line # 29

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
1	silicon	7.7890	.0100	.00	221	1000	<100>

Integrated Dopant (#/cm**2)

layer no.	Net active	Net chemical	Sum active	Sum chemical
1	3.2652E+15	3.7206E+15	3.2652E+15	3.7206E+15
sum	3.2652E+15	3.7206E+15	3.2652E+15	3.7206E+15

Integrated Dopant (#/cm**2)

layer no.	phosphorus active	phosphorus chemical
1	3.2652E+15	3.7206E+15
sum	3.2652E+15	3.7206E+15

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (#/cm**2)	sum chemical Qd (#/cm**2)
1	1	n	-.0001	7.7890	3.2678E+15	3.7240E+15

Fig. 7.5. Continued.

```
1
 Sheild using the wafer without doping-Cross AA
 SOURCE

 Electrical information
 Input line #  30


 Bias step   1


 layer region type  Conductor Bias  Electron Bias   Hole Bias
  no.    no.            (volts)        (volts)       (volts)
   1      1     n                    0.0000E+00    0.0000E+00


                Electron Charge, Conductance, and Resistance

                    Electron       Sheet        Sheet       Vertical
Vertical
 layer region type   Charge     Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))  (ohm/sq)    (mho/cm**2) (ohm-
cm**2)
   1      1     n  3.266E+15   3.2422E-02  3.0843E+01   3.7306E+02
2.6806E-03


                  Hole Charge, Conductance, and Resistance

                     Hole         Sheet        Sheet       Vertical
Vertical
 layer region type   Charge     Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))  (ohm/sq)    (mho/cm**2) (ohm-
cm**2)
   1      1     n  0.000E+00   0.0000E+00                0.0000E+00


 *** END SUPREM-3 ***
```

Fig. 7.5. Continued.

```
*************************************************************
***                        SUPREM-3                       ***
***                  Version P, Revision 9002             ***
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***         Technology Modeling Associates, Inc.          ***
***                  All Rights Reserved                  ***
***                                                       ***
***          Licensed to Iowa State University            ***
***                  Serial # 0155401845                  ***
*************************************************************

                        3-Aug-96 15:37:58

     Statements input from file sheild


    1... Title   Suprem-III Sheild with low resistivity
    2... $Let us start with a <100> silicon substrate with initial
    3... INITIALIZE       SILICON<100> Phosphors=1.5e15
     ... +       THICKNESS=8.0   DX=0.01
    4... SOLUBILITY       BORON SILICON TEMPERATURE
     ... +       TABLE=(700, 800, 900, 1000, 1100, 1200)
    5... SOLUBILITY       BORON SILICON SOLUBILITY
     ... +       TABLE=(9E19, 28E19, 30E19, 34E19, 37E19, 40E19)
    6... IMPURITY         BORON SILICON DIP.0=3.5E9
    7... SEGREGATION      BORON SILICON /AMBIENT TRANS.0=5.5 TRANS.E=1.0
    8... SEGREGATION      BORON SILICON /OXIDE SEG.0=104 SEG.E=0.66
    9... COMMENT OPTIONAL ENHANCEMENT DURING SOAK ONLY
   10... IMPURITY         BORON SILICON TED.0=1E-3 TED.E=-0.8 TED.TAU=10
TED.CONC=1E20
   11... IMPURITY         PHOSPHORS SILICON NE.0=5.0E21 CTN.F=2.85 DIM.0=14E9
     ... +       DIMM.0=4.5E11
   12... SEGREGATION      PHOSPHORS SILICON /AMBIENT TRANS.0=9.5 TRANS.E=0.7
   13... SOLUBILITY       PHOSPHORS SILICON Temperature
     ... +       TABLE=(700, 800, 900, 1000, 1050, 1100)
   14... SOLUBILITY       PHOSPHORS SILICON SOLUBILITY
     ... +       TABLE=(12E19, 42E19, 55E19, 10E19, 12E19, 13E20)
   15... Comment Start with the bare wafer
   16... COMMENT BEGIN N DIFFUSION
   17... COMMENT PREDEPOSITION
   18... COMMENT SOURCE
   19... DIFFUSION      Temperature=900 TIME=40 ss.PHOSP UD.PHOSP NITROGEN
   20... PRINT LAYER
   21... PRINT ELECTRICAL
   22... COMMENT GROW OXIDE
   23... Diffusion       Temperature=800 Time=19 T.RATE=16 NITROGEN
   24... Diffusion       Temperature=1100 Time=36 WETO2
   25... Diffusion       Temperature=1100 Time=70 T.RATE=-4.1 NITROGEN
   26... PRINT   LAYER
   27... PLOT    ACTIVE PHOSPHORS COLOR=1 pause
```

Fig 7.6. Suprem simulation of fabrication process for structures shown in Fig. 7.1.B.

```
  28... PRINT LAYER
  29... PRINT ELECTRICAL
  30... STOP
```

```
 Input line #   3
 Coefficient data group read
 File: \tma\s3_9002\library\s3cof0
 Date:  8-Jul-96 13:34:45
 Documentation from data file:

 SUPREM-3 Revision 9002 coefficient initialization

1
 Suprem-III Sheild with low resistivity
 SOURCE

 Material layer information
 Input line #  20


 layer  material      thickness    dx       xdx   top bottom  orientation
  no.                    (um)     (um)     (um) node  node  or grain size
   1    silicon         8.0000    .0100     .00  200  1000       <100>

                  Integrated Dopant (#/cm**2)
 layer              Net                          Sum
  no.      active       chemical       active       chemical
   1     5.1510E+15   5.9748E+15   5.1510E+15   5.9748E+15
  sum    5.1510E+15   5.9748E+15   5.1510E+15   5.9748E+15

                  Integrated Dopant (#/cm**2)
 layer          phosphorus
  no.      active       chemical
   1     5.1510E+15   5.9748E+15
  sum    5.1510E+15   5.9748E+15

               Boundary Locations and Integrated Dopant
               Concentrations for Each Diffused Region
 layer  region  type       top        bottom        net            sum
  no.     no.              depth       depth     active Qd     chemical Qd
                           (um)        (um)      (#/cm**2)      (#/cm**2)
   1       1      n      -.0001      8.0000    5.1540E+15     5.9787E+15
```

Fig 7.6. Continued.

```
1
 Suprem-III Sheild with low resistivity
 SOURCE

 Electrical information
 Input line #  21


 Bias step   1


 layer region type  Conductor Bias  Electron Bias   Hole Bias
  no.    no.            (volts)        (volts)       (volts)
   1      1     n                   0.0000E+00    0.0000E+00


                Electron Charge, Conductance, and Resistance

                    Electron      Sheet       Sheet      Vertical
Vertical
 layer region type   Charge    Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))  (ohm/sq)   (mho/cm**2) (ohm-
cm**2)
   1      1     n  5.151E+15   4.9486E-02  2.0208E+01   3.8083E+02
2.6258E-03


                  Hole Charge, Conductance, and Resistance

                      Hole        Sheet       Sheet      Vertical
Vertical
 layer region type   Charge    Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))  (ohm/sq)   (mho/cm**2) (ohm-
cm**2)
   1      1     n  0.000E+00   0.0000E+00               0.0000E+00
1
 Suprem-III Sheild with low resistivity
 GROW OXIDE

 Material layer information
 Input line #  26


 layer  material      thickness   dx      xdx  top bottom  orientation
  no.                    (um)     (um)    (um) node  node  or grain size
   2     oxide           .5519    .0100   .00  198   223
   1     silicon        7.7572    .0100   .00  224   1000       <100>

                Integrated Dopant (#/cm**2)
```

Fig 7.6. Continued.

```
 layer              Net                          Sum
  no.       active        chemical       active        chemical
   2     2.9280E+14    2.9280E+14    2.9280E+14    2.9280E+14
   1     2.8393E+15    2.8457E+15    2.8393E+15    2.8457E+15
  sum    3.1321E+15    3.1385E+15    3.1321E+15    3.1385E+15

                  Integrated Dopant (#/cm**2)
 layer           phosphorus
  no.       active        chemical
   2     2.9280E+14    2.9280E+14
   1     2.8393E+15    2.8457E+15
  sum    3.1321E+15    3.1385E+15

               Boundary Locations and Integrated Dopant
               Concentrations for Each Diffused Region
 layer  region  type       top         bottom          net             sum
  no.     no.              depth        depth      active Qd      chemical Qd
                           (um)         (um)       (#/cm**2)       (#/cm**2)
   2       1      n        .0000        .5519     2.9280E+14     2.9280E+14
   1       1      n       -.0001       7.7572     2.8396E+15     2.8460E+15
1
 Suprem-III Sheild with low resistivity
 GROW OXIDE

 Material layer information
 Input line #  28


 layer  material       thickness    dx       xdx   top  bottom  orientation
  no.                     (um)      (um)     (um)  node   node  or grain size
   2     oxide             .5519    .0100     .00   198    223
   1     silicon          7.7572    .0100     .00   224   1000       <100>

                  Integrated Dopant (#/cm**2)
 layer              Net                          Sum
  no.       active        chemical       active        chemical
   2     2.9280E+14    2.9280E+14    2.9280E+14    2.9280E+14
   1     2.8393E+15    2.8457E+15    2.8393E+15    2.8457E+15
  sum    3.1321E+15    3.1385E+15    3.1321E+15    3.1385E+15

                  Integrated Dopant (#/cm**2)
 layer           phosphorus
  no.       active        chemical
   2     2.9280E+14    2.9280E+14
   1     2.8393E+15    2.8457E+15
  sum    3.1321E+15    3.1385E+15
```

Fig 7.6. Continued.

```
                Boundary Locations and Integrated Dopant
                Concentrations for Each Diffused Region
 layer   region  type      top       bottom       net           sum
  no.      no.            depth       depth     active Qd     chemical Qd
                          (um)        (um)      (#/cm**2)      (#/cm**2)
   2        1       n      .0000       .5519    2.9280E+14     2.9280E+14
   1        1       n     -.0001      7.7572    2.8396E+15     2.8460E+15
1
 Suprem-III Sheild with low resistivity
 GROW OXIDE

 Electrical information
 Input line #  29


 Bias step   1


 layer region type  Conductor Bias  Electron Bias    Hole Bias
  no.    no.             (volts)        (volts)        (volts)
   1      1      n                    0.0000E+00     0.0000E+00


                Electron Charge, Conductance, and Resistance

                    Electron       Sheet        Sheet       Vertical
Vertical
 layer region type   Charge     Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))   (ohm/sq)   (mho/cm**2)  (ohm-
cm**2)
   1      1      n  2.840E+15   4.3983E-02  2.2736E+01   4.4462E+02
2.2491E-03


                  Hole Charge, Conductance, and Resistance

                      Hole         Sheet        Sheet       Vertical
Vertical
 layer region type   Charge     Conductance  Resistance  Conductance
Resistance
  no.    no.        (#/cm**2)  (1/(ohm/sq))   (ohm/sq)   (mho/cm**2)  (ohm-
cm**2)
   1      1      n  0.000E+00   0.0000E+00                0.0000E+00


 *** END SUPREM-3 ***
```

Fig 7.6. Continued.

Experimental results and related discussion

After fabrication of the structures shown in Fig. 7.1, a network analyzer is utilized to measure S_{12}. To do that we connect parallel lines in one side of the wafers to one port of a network analyzer and the parallel lines in the other side of the wafer to the other port of a network analyzer.

The measured S_{12} for the first and second set of wafers are presented in Fig. 7.7. Also the power ratio transmitted $|S_{12}|^2$ is presented in Fig. 7.8. There are two observations can be made from these figures. First, the fact that this type of shielding is highly effective. As it can be seen from Fig. 7.8, the transmitted power to the second set of lines is less then 5% at it's peak. This is a good news for our research. It means an extremely effective shield can be made using the method described in chapter 2.

Also it can be noted that the transmittance curve in Fig. 7.8 is not flat, as it is predicted in Chapter 2. The reasons for this fact are the frequency dependence of the connecting network to the network analyzer, frequency dependence of the test structure itself, radiation pattern characteristics of the test structure, and the fact that carrier electrons inside the shield have inertia and impose a reactive term on bulk resistivity of the wafer.

The inductive term can arise from the fact that the electrons and holes have finite masses. Therefore, when the direction of the field is changed the carries continue moving in the direction they were moving and create an inductive like effect. Therefore the resistivity of a semiconductor should be expressed in terms of real and imaginary parts.

To understand the mathematics of this phenomenon let us consider the energy of the carriers. Let us assume the majority carriers are electrons. Then we can write:

$$-eE - m\frac{\upsilon}{\tau} = m\frac{\partial \upsilon}{\partial t} \qquad \text{Eq. 7.3}$$

Assuming the velocity change is sinusoidal

$$v = v_o \exp(j\omega t) \quad \text{Eq. 7.4}$$

Then, it can be written:

$$\frac{\partial v}{\partial t} = j\omega v_o \exp(j\omega t) \quad \text{Eq. 7.5}$$

Substituting in Equation 7.3 we get:

$$-eE - m\frac{v}{\tau} = jm\omega v \quad \text{Eq. 7.6}$$

Therefore:

$$v = \frac{-eE\tau}{m(1 + j\omega\tau)} \quad \text{Eq. 7.7}$$

On the other hand conductivity is defined by:

$$\sigma = \frac{J}{E} \quad \text{Eq. 7.8}$$

Where J is given as:

$$J = -n\,ev \quad \text{Eq. 7.9}$$

as a result resistivity can be shown to be:

$$\rho = \frac{1}{\sigma} = \frac{m(1 + j\omega\tau)}{n\,e^2\tau} = \rho_o(1 + j\omega\tau) = \frac{m}{n\,e^2\tau} + j\frac{m\omega}{n\,e^2} \quad \text{Eq. 7.10}$$

This shows that the resistivity of semiconductors has a reactive part, which partially explains the difference between the experimental results and the theoretical results obtained with the assumption that the resistivity of the semiconductor material is purely resistive. Never the less, the experiment proves that an effective shield can be made using this method.

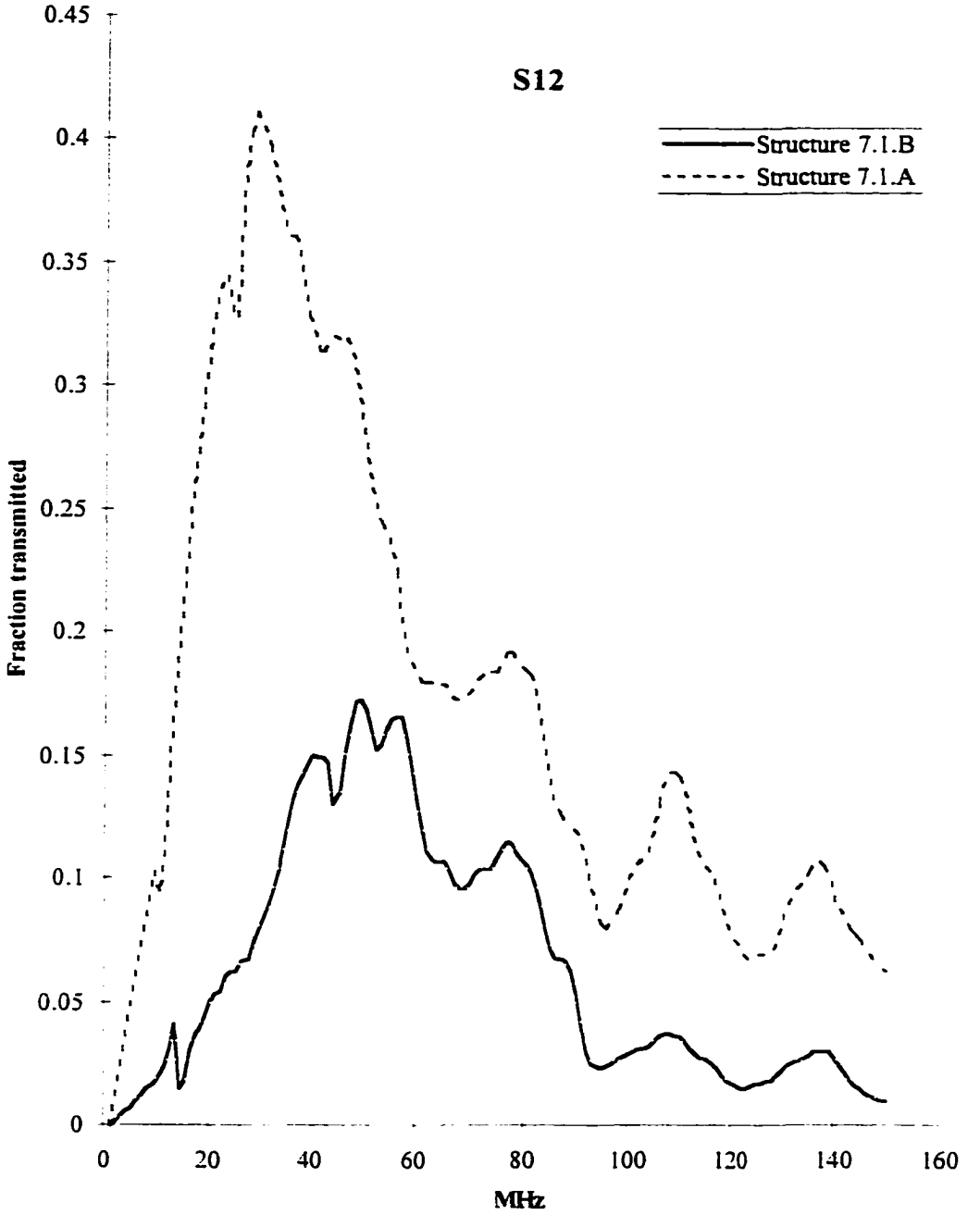


Fig. 7.7. S_{12} measured for structures shown in figures 7.1

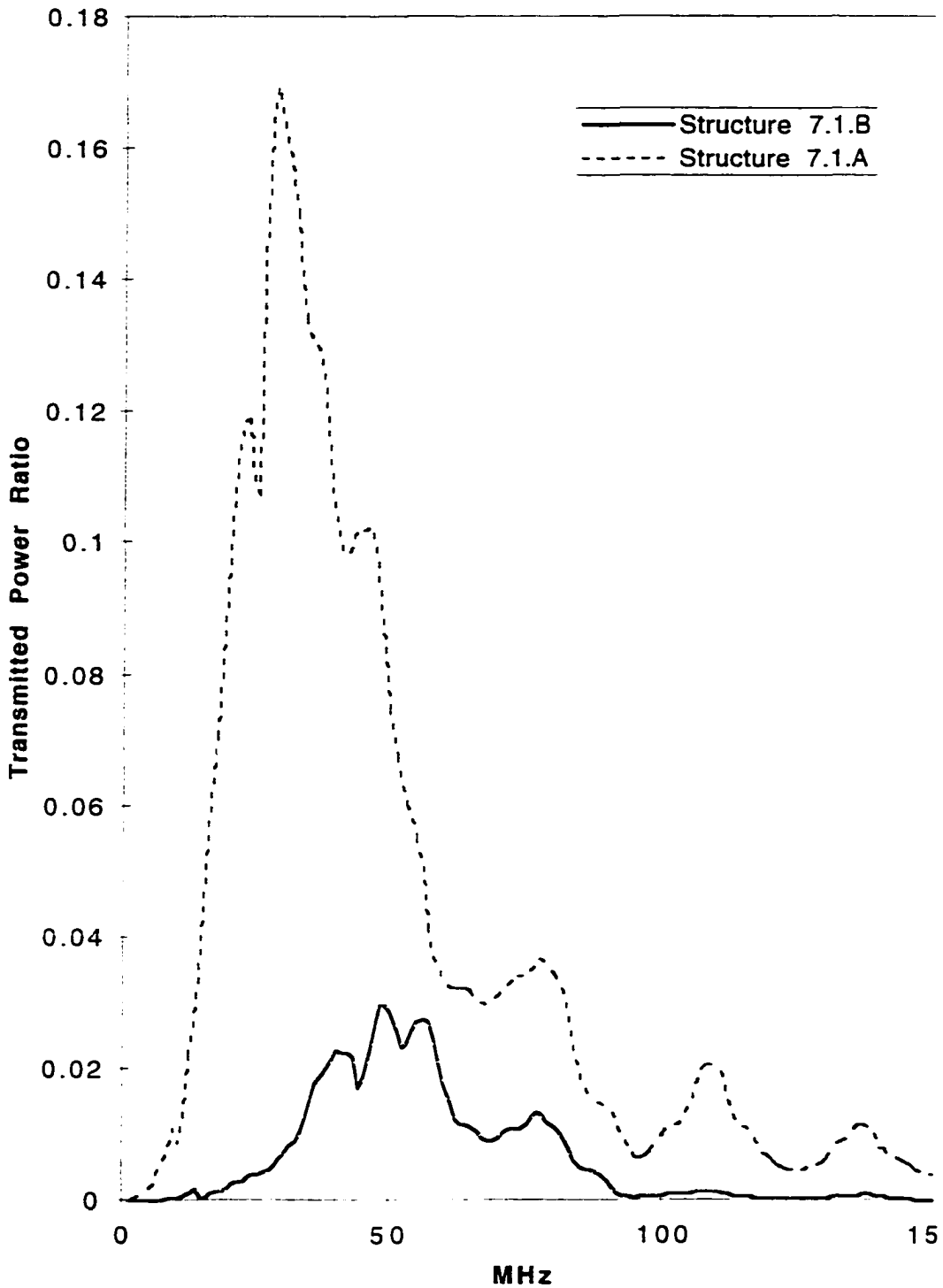


Fig. 7.8. The power transmitted to the second set of the lines on the other side of the wafers.

CONCLUSIONS

Our intention in this work was to develop a practical 3DI technology by resolving associated problems.

One of our important contributions to this field is the solution to the problem of cross-talk between closely packed layers. This is done by introducing a heavily doped semiconductor shield layer in between the stacked 3DI layers. A theoretical analysis of this inter-layer shield is presented in Chapter 2. This analysis suggests that the problem of cross-talk between closely packed layers in a 3DI technology can be effectively managed using an inter-layer semiconductor shield. Further more, this study suggests that a highly effective and reletively thin shield can be fabricated to manage the problem of cross-talk. The effectiveness of an inter-layer shield in integrated circuit environment, the analysis reveals, is mainly related to the material conductivity of the shield.

To test this theoretical findings, we manufactured two sets of semiconductor wafers. Both sets had the same thickness; however, we diffused a heavy dose of impurities a few μm deep in one set of wafers to create a highly conductive region. Then we oxidized the wafers and created adjacent parallel lines on both sides of the wafers. Using a network analyzer, the S_{12} of both sets of wafers were measured. This measurement showed that the set of wafers with higher conductivity region was far more effective in reduction of cross talk. Further more, this few μm thick layer effectively reduced the cross talk problem to a negligible value. The full detail of the experimental work related to inter-layer shield is presented in Chapter 7.

Another important contribution of this paper is introduction of a new architecture for active devices that are more suitable for incorporation into a 3DI technology in Chapter 1. This new device has only one type of impurity. Having only one type of impurity region in a device enables the device to better resist the heating process associated with fabrication process. Further more this device takes full advantage of the layered SOI nature of 3DI technology. The

practical consideration in choice of materials for functionality of this device is described in Chapter 5. This chapter suggests that Sb-Au alloy should be used as an ohmic contact for n-type silicon and Al should be used as an ohmic contact for p-type silicon. This is later verified using computer simulation at the end of Chapter 6.

To complete this work, we have suggested a new manufacturing process in Chapter 3. The manufacturing process incorporates sophisticated processing steps, such as crystal seeding, laser recrystalization, sacrificial etch back planarization, and other low temperature processing techniques. These technologies are reviewed in Appendix 1. This process is verified by SUPREM computer simulation in Chapter 6.

APPENDIX: A BRIEF REVIEW OF RELATED MATERIALS

A BRIEF REVIEW OF RELATED MATERIALS

One of the best ways to start any subject is by going to its roots and history. Through this tactic, readers can become familiar with the required backgrounds needed to follow the subject. One can then present the problems that hinder further progress and propose a solution for them. With these goals in mind, an attempt has been made in the next section to briefly follow the development of semiconductors and its fabrication technology giving particular emphasis to issues that relate to the subject at hand. Moreover, this section intends to establish the industry's need for development of Three Dimensional Integration(3DI) of semiconductors.

A.1 Historical Review

Although, semiconductor devices had been in use as early as the late nineteenth century; World War II was credited as the driving force for the development of the semiconductor industry as we know it today. If the armed forces involved in that war had not required need for a small and portable electronic equipment, the intense race for the development of a "solid state tube" might not have taken place. This intense race finally resulted in the invention of the first transistor in Bell laboratories after the conclusion of that bloody war. The first technical paper regarding this invention was published by J. Bardeen and W. H. Brattain[46]. Soon after this, William Shockley published his classic paper: "The theory of p-n Junctions in Semiconductors and p-n Junction Transistors"[47].

Shortly after the research team in the Bell Laboratories invented the transistor in the late 1940's, Jack Kilby, a young engineer at Texas Instruments, was able to realize the first monolithic semiconductor integrated circuit in 1958.[48] Although, the credit should also given to G. W. A. Dummer who was the first person to publicly suggest that electronic equipment could be made "in a solid block with no connecting wires. The block may consist of layers of insulting, conducting, rectifying and amplifying materials, the electrical function being

connected directly by cutting out areas of various layers"[49]. His suggestions probably had great influence on many people of his time. Just a few months after Kibly's work on Germanium, Robert Noyce independently announced a silicon based technology which had close resemblance to today's silicon technology[48]. These two technologies later joined with others, which are based on other semiconductors such as GaAs or InP, to form the bases of today's semiconductor technology.

Early integrated circuits consisted of just a few devices. However, in the early stages of the development in this industry, the number of devices per chip doubled each year. The rapid trend toward miniaturization was first fueled by the military's need for smaller and ever more sophisticated electronic circuits. Later on, it was observed that large scale production of integrated circuits is more cost efficient than other methods of production. Therefore, in order to produce lower cost products, more and more devices were integrated inside one chip. Up to present time, the increases in the integration density were mainly due to reduction in the device size, or an increase in the area allocated per chip.

Since the early days of semiconductor technology, dramatic changes have taken place in the basic technology of the integrated circuit manufacturing. Most of these changes have been made to:

- Achieve higher quality.
- Increase the yield of the processes involved in production of integrated circuits.
- Make the overall circuit faster.
- Solve the physical problems of integrating more devices per chip.
- Overcome the technological problems of integrating more devices per chip.

Four fully distinguishable classes of fabrication technology have replaced each other. SSI (Small Scale Integration) in the late 1950's and the early 1960's, MSI (Medium Scale Integration) of the late 60's, and LSI (Large Scale Integration) of the 1970's that was finally

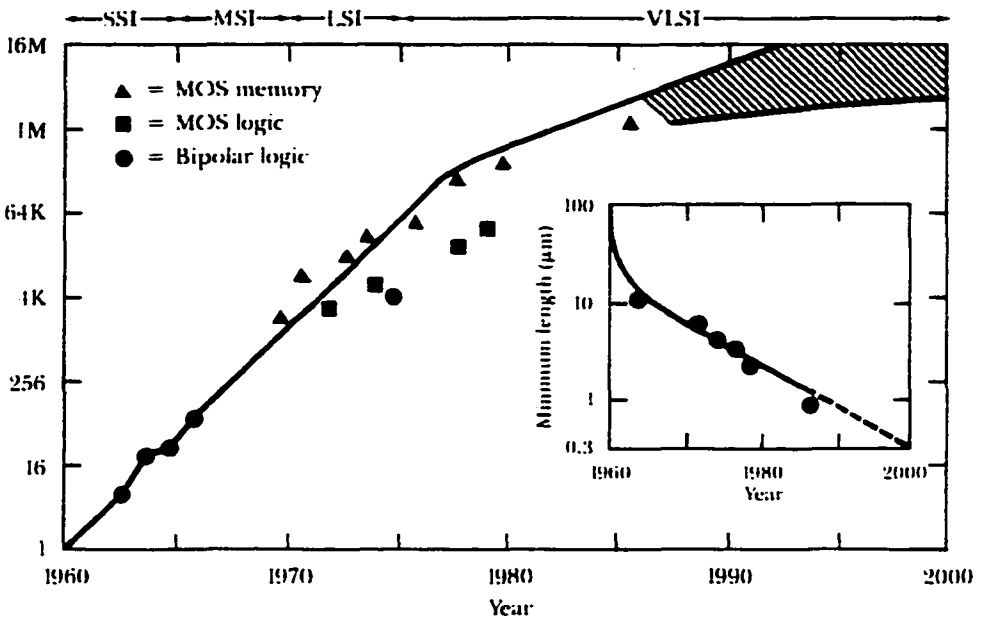


Fig. A.1. Growth in number of devices per chip. The graph has been extrapolated for the 1985 to the year 2000. Also the reduction in device size is shown in lower right corner of the Fig. A.1[50]

replaced with the currently used VLSI (Very Large Scale Integration) technology. The exponential increase in the number of devices integrated per chip since the early developmental stages of the semiconductor industry is shown in Fig. A.1. This figure also projects the expected increase of integrated devices per chip until the year 2000.

A.1.1. Bipolar vs. Field Effect Transistor

The earlier technologies had mainly focused on bipolar devices as the workhorse for implementing an electrical circuit; whereas, the later technologies have shifted their attention from Bipolar devices toward Field Effect Transistors (FET) as the main active element. The

shift in attention from bipolar to FET was due to several reasons. Among the most important ones was the fact that FETs can be made in smaller sizes than bipolar transistors.[51] This is partly due to the fact that the smaller the emitter surface area in a bipolar transistor, the larger it's resistance. This resistance not only creates a negative feedback loop, which decreases the gain by itself, but also contributes to over all base resistance, further decreasing the gain of a transistor. Other motivations for industry's reorientation from bipolar transistors to FETs can be observed by comparing the scaling relationships for these two devices. Table A.1 shows the scaling relationship for both MOSFETs and bipolar transistors[52-54].

Table A.1. Scaling relationship[52].

Device Parameter	Bipolar[72]	MOS[21]
Device dimensions L,W,d	1/S	1/S
Doping concentration, N.	1	S
Oxide thickness X_o	1/S	1/S
Junction depth X_j	1/S	1/S
Voltage V	1	1/S
Current I	$1/S^2$	1/S
Capacitance C	$1/S^2$	1/S

Change in the performance of these devices as a result of the scaling is shown in Table A.2.[55] As shown in this table, the speed improvement for an scale down MOSFET is more noticeable than a bipolar transistor. This is as a result of the fact that speed and other performance characteristics of a MOSFET are more dependant in the horizontal geometry of the

device, since normally MOSFETs are built horizontally; whereas, the performance of a bipolar transistor is more affected by vertical geometry. Contrary to MOSFET, the most popular way to built a bipolar transistor is by diffusion of different impurities vertically into the surface of the wafer. Although, it is possible to built the bipolar transistor horizontally; for such horizontally built transistors to function well, one must allocate ample space to the emitter.

It worth mentioning that power is reduced by a factor of $1/S^2$ for both devices; even though, power density remains constant. This indicates that no advantage could be gained in terms of circuit cooling by scaling down these devices. However, it is noticeable that the speed power product has been reduced more for MOSFET ($1/S^3$), than for bipolar transistor ($1/S^2$). This is due to greater speed improvement for MOSFET.

Table A.2. Speed power comparison.[55]

Parameter	Bipolar	MOS
Delay time $\tau=C(\Delta V/I)$	1	1/S
Power = VI	$1/S^2$	$1/S^2$
Power density = VI/A	1	1
Speed X Power = $VI\tau$	$1/S^2$	$1/S^3$

Finally, it should be noted that in the bipolar transistor, even with reduction in emitter size, the overall size of the transistor tends to be large[55]. Moreover, any reduction in the emitter size results in an increase of the base resistance of the transistor itself, which in turn reduces the gain of the transistor as mentioned already. Table A.3 presents a summary of the characteristics of bipolar and MOSFET transistors of different sizes for comparison purposes[56].

Table A.3. Device characteristics.[56]

Bipolar	Emitter Size W * L (μm)		
	2.5 X 5.0	0.5 X 1.0	0.25 X 0.25
W_B(μm)	0.1	0.1	0.1
$\tau=W^2/2D$ sec, D~10 cm^2/sec	$5X10^{-12}$	$5X10^{-12}$	$5X10^{-12}$
I(A)	10^{-3}	$4X10^{-5}$	10^{-5}
$Q = I\tau$ (C)	$5x10^{-15}$	$2X10^{-16}$	$5X10^{-17}$
$C_D = Qq/kT$ (F)	$2X10^{-13}$	$8X10^{-15}$	$2X10^{-15}$
$g_m = C_D/\tau$ (mho)	$4X10^{-2}$	$1.6X10^{-3}$	$4X10^{-4}$
MOSFET	Channel Size L*W (μm)		
	2.5 X 5.0	0.5 X 1.0	0.25 X 0.25
X_o (A^o)	700	140	70
$\tau = L / v_s$ (sec)	$25X10^{-12}$	$5X10^{-12}$	$2.5X10^{-12}$
$C_G = WLC_o$ (F)	$6X10^{-15}$	$1.2X10^{-15}$	$6X10^{-16}$
I (A)	10^{-4}	$2X10^{-5}$	10^{-5}
$Q = I\tau$ (C)	$2.5X10^{-15}$	10^{-16}	$2.5X10^{-17}$
$C_c = Qq/kt$ (F)	10^{-13}	$4X10^{-15}$	10^{-15}
$C_{eq} = C_G C_C / (C_G + C_C)$(F)	$\sim 6X10^{-15}$	$9.23X10^{-16}$	$3.75X10^{-16}$
$g = C_{eq} / \tau$ (mho)	$2.4X10^{-4}$	$1.85X10^{-4}$	$1.5X10^{-4}$

A.1.2. The Limits of Current Technologies

If one looks back to Fig. A.1 once again, one will notice that the increase in integration density has been slowing. This phenomenon is mainly due to the fact that even the MOSFETs are reaching their lowest miniaturization limit[57], which physics of the device permits.

Even though, MOSFETs are better suited for miniaturization than bipolar transistors are; they have their own scaling limitations as well[57]. Among the problems that should be considered in designing a MOSFET in submicron range are[58]:

1. Hot carrier injection into the gate oxide, which results in threshold voltage instability.

2. Avalanche breakdown as result of high doping density. (This high level of doping density are desirable to keep the depletion region of the source and drain as small as possible in order to have shorter gate lengths).

3. Electric breakdown in thin oxide thicknesses.

4. Short channel and narrow gate effects, which increase the threshold sensitivity to even a small manufacturing process variations.

5. Increase in subthreshold current. This current does not scale down with the rest of the currents in the device; therefore, it constitutes the larger portion of the total current in sub-micron range.

6. Latch-up, which is as a result of interaction between two closely located MOSFETs on single crystal wafer technology; even though, this problem does not exist in SOI technology.

In addition, the statistical nature of substrate characteristics (such as distribution of impurities[57], surface condition[59], fixed and mobile charges[60] of the oxides which vary slightly from location to location in the substrate[61]) result in much larger and more significant variations in the smaller dimensions[1].

---

[1] To better understand the significance of this statestical distribution of impurities in a small dimensions[57], let us assume that doping density of semiconductor is N; therefore, total number of atoms located in a cube of size D is given by:

$$M = ND^3 \quad \boxed{\text{Eq. F1}}$$

where M is average number of impurities found in a cube. For example, $N = 2X10^{15}cm^3$ will result in 2 impurity atoms in a cube with $D=10^{-5}$ cm (0.1 μm). However, this is an average number and this cube could hold any where from 1 to 3 impurity atoms. This in turn for a device with dimension of 0.1 μm translates to doping density of:

$$N = \frac{M}{D^3} = \frac{3}{10^{-15}} = 3X10^{15}\ \text{atoms/cm}^3 \quad \boxed{\text{Eq. F2}}$$

To

$$N = \frac{M}{D^3} = \frac{1}{10^{-15}} = 1X10^{15}\ \text{atoms/cm}^3 \quad \boxed{\text{Eq. F3}}$$

Since many charcterestics of our device are related to doping density, a change of this magnitude might cause some of the devices to malfunction. Therefore, the overall yeild of manufacturing drops fast. Similar conclusion could be drawn for the variation in other substrate properties.

A.1.3. Introduction of Submicron Devices

To circumvent these problems, several new devices have been proposed[62-67]. These new devices were specially engineered with the consideration of the problems mentioned above, so they would be able to function in sub-micron range. This trend to design new devices that could work in sub-micron range, was among the first attempts by a group of researchers done to increase the density of the devices per chip for future generations of fabrication technologies. The technology that utilizes this approach to achieve higher degree of integration is commonly known as Ultra Large Scale Integration or ULSI. These researchers have developed many such devices and design fabrication procedures to manufacture them[62-67]. Devices such as VMOS[62], UMOS[63], DMOS[64], DIMOS[65], and SB-IGFET[67] are a few examples of their results. However, all these methods require additional processing on the wafer, which reduces the manufacturing yield and complicates the manufacturing process. Moreover, there are important lithographical constraints that need to be considered. As the device size decreases beyond 0.05 μm, the electron should also be considered as a particle with all its quantum mechanical properties. Therefore, this fact establishes a lower limit on how small a device can become without running into the quantum mechanical effects. A paper on the quantum mechanical limitation of a digital device has been presented by R. T. Bate[68].

However, special devices have been engineered with full consideration of the quantum mechanical properties of electrons[69-73]. These devices fully utilize the quantum mechanical properties of electrons to provide even more superior characteristics than regular devices[70]. SDHT, TEGFET, HEMT, MODFET, Quantum Wells, and other Bandgap Engineered active elements are good examples of such devices[69-73]. Nevertheless, in order to fabricate these devices with current technology a large area on the wafer should be allocated to each device (in order of one or two microns) .

A.1.4. Lithographical Considerations

The development of the lithography has been very important to the work of these and other researchers, since lithography could be considered to be one of the limits in miniaturization[74-75]. Therefore, it is prudent to look into the development of lithography and its current state of art in more detail.

A.1.4.1. Optical Lithography

Today's optical lithography, a mixture of an ancient and a modern art, is considered to be the oldest form of lithography in existence[76]. Although, most techniques of this art has been developed and perfected during past 30 years; the photoresist process itself was developed 150 years ago for photoengraving by Niepce[77]. Going still further back in time, one of the first works in microphotography was done in 1839 by Dancer[78]. It was in the 1950s that this technique was adopted for thin-film and printed circuit board applications. A few years later in the 1960s, this technology with the use of "the photoresists developed for printed circuits"[76], established itself as one of the essential companents of almost all fabrication technologies[76].

Since then, optical lithography has gone through enormous changes. Prior to 1970, the tools for lithographic exposure were evaluated by the term "resolution"[76]. For example, "a 10-μm machine" meant that the smallest realizable line-width with an ideal exposure conditions was 10 μm. At about this time, around 1970, fabrication engineers were advised that minimum resolution is not relate to the "performance under manufacturing conditions"[76]; therefore, new terms such as "minimum feature size" and "minimum working feature" were invented to describe the smallest achievable feature with a reasonable yield[76].

By development of 4.0 μm feature size technology in 1975[76], a single parameter was no longer sufficient to describe lithographical performance of a technology. It was noted

that technologies providing smallest feature sizes did not necessarily perform satisfactorily for larger features of a device[79]. Meanwhile, demand for better control on overlay accuracy and line-width control in long lines could not be met by some of lithographic exposure equipment capable of producing very small feature sizes.[79] Therefore, the expression "minimum feature size of x micrometers" had added meaning that the exposure tools satisfy all required characteristics of x micrometer design rules[79].

The advent of 2.0 μm design rules in 1979 made it too difficult to evaluate the lithographical performance without full consideration of non-hardware aspects of the technology[79]. Today, three criteria of a photolithographical technology are evaluated[79]. The first criterion is the "aerial image" or the optical quality of technology without consideration of resist or the process. Second one is the effects of the resist on the image, i.e., the resist profile after development. Finally, the quality of the image over entire wafer, including such things as line-width variations and the accuracy in placement of features on the wafer are considered. These concepts are demonstrated in Fig. A.2[80].

A.1.4.2. Other Forms of Lithography

Ultimately, the lithography's resolution is limited to the wave length of the emitting source of the system; that is, the generated patterns can notbe much smaller than the wave length of the a emitting source. Thus, optical lithography is limited to around 0.5 μm. Therefore, for the higher resolutions emitting sources with shorter wave length should be utilized. This led to introduction of UV and X-ray lithography[81-82]. However, at shorter wave lengths, many masks used for photolithography do not function. This is due to the fact that some transparent materials to the light are opaque to the X-ray radiations, and vice versa.

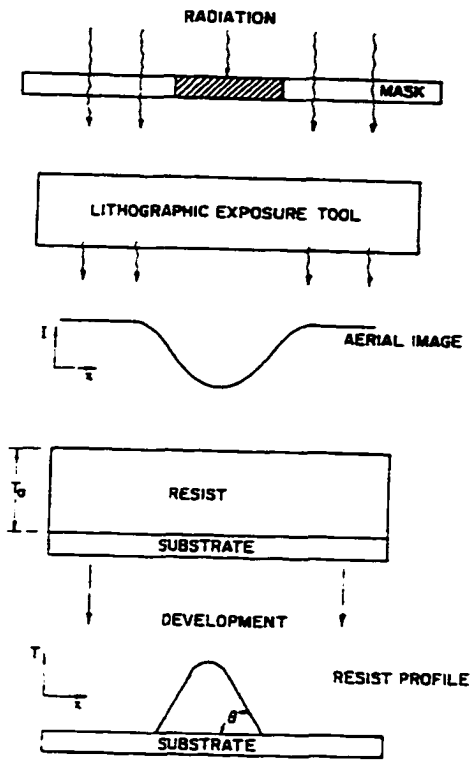


Fig. A.2. An Idealized photolithographic system[80].

Alternatively, other sources such as electrons or ions could be used in place of electromagnetic emitting source in a lithographical system. After all, electrons and ions show wave properties in a quantum mechanical view of the world. Utilization of these two sources led to introduction of Electron-Beam Lithography[83] and Ion-Beam lithography[84]. Yet there are limitation on resolution of these types of lithography, as well[85]. Moreover, Electron-Beam and Ion-Beam lithography can cause radiation damage. Fig. A.3 presents a visual description of all these different forms of lithography and Fig. A.4 is a comparative graph of approximate resolution of these lithographical technologies[86][87].

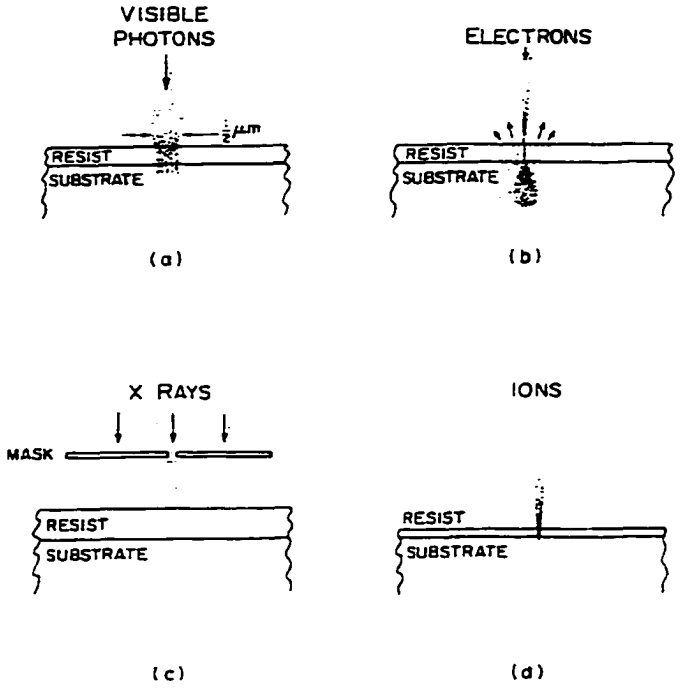


Fig. A.3. "Types of advanced lithographies for submicron structure fabrication. (a) Photo-lithography. the mainstay of the microelectronics industry, is used routinely down to 2 to 3-μm linewidths; the practical limit may approach 0.5 μm. (b) Electron-Beam lithography, which has produced microstructures on thin films below 100 'A. Suffers from backscatter electrons on bulk substrates when the patter elements are closer than 0.5 μm . (c) X-ray lithography is very effective to near 100 'A but requires a relatively thick absorber-mask pattern on a thin supporting membrane. (d) Ion-beam lithography offers a tremendous potential for very high resolution microstructure fabrication because of very large energy dissipation near surface and the short range of secondary excitation processes."[86]

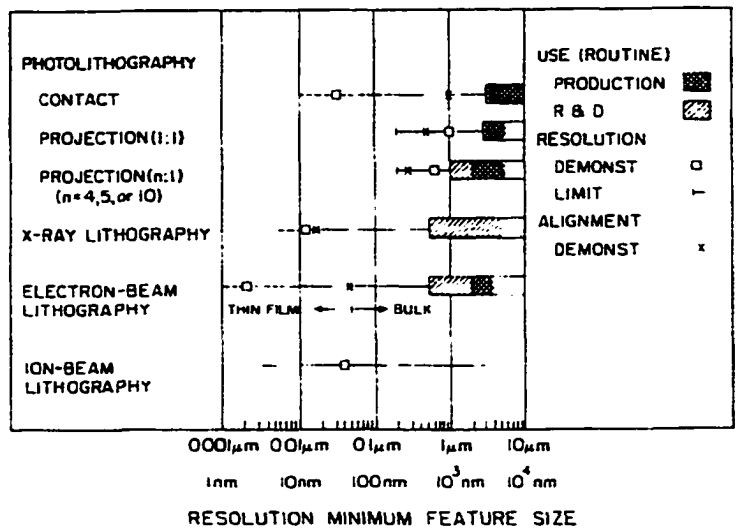


Fig. A.4. A compression among four different types of lithography.[87]

A. 1.1.5. Wafer Scale Integration (WSI)

In order to increase the number of devices per chip, another group of researchers are currently exploring ways to enlarge the area allocated per each chip (die size) on a wafer. Their efforts are mainly concentrated in finding ways to improve the yield factor for fabrication processes of large die sizes. Wafer Scale Integration (WSI) is becoming possible as a result of efforts in this branch of research.

One of the most challenging aspects of these new technologies is their tolerance for manufacturing defects. These defects are either originally present on the wafer itself from the very beginning, or resulted from one of the several processing procedures performed on the wafer. Therefore, without a mechanism for fault tolerance, the yield factor falls to such an unacceptable level that practically no working wafer could be produced. As a result, efforts are concentrated to develop various mechanisms for fault tolerance[88].

The most promising approach in this area is to divide the entire system into several smaller modules. These modules is then grouped into several identical sets. In each wafer, additional number of modules are fabricated. Finally, the defective modules are rewired out of the whole system and the signal is rewired to axillary modules by blowing up the fusses in the signal path[74-75,85]. This method has been proven to be very effective for digital circuitry[88].

Of course, the problem that eventually limits this technology is the size of the wafer itself. The size of wafer is currently limited to several inches at most. Even if the larger wafer sizes become available, it might not be practical from the consumer stand point to fabricate a whole system on a big dish the size of a 12' satellite antenna! However, it should not be forgotten that currently the largest available wafers have a diameter of less than 1 foot long. Therefore, this limitation will eventually makes this technology obsolete. Nevertheless, WSI might provide an intermediate technology in the near future.

A.2. Introduction to 3DI and Related Technologies

To further increase the device density in a chip a suggestion was made, in this paper to construct the circuits on several Semiconductor On Insulator Layers (SOI). These layers could be stacked on top of each other to form a Three Dimensionally Integrated (3DI) circuit. This way, the device density of an integrated circuit could be increased with or without reduction in the device size. However, several technologies should be developed before Three Dimensional Integration can become a reality. Let us briefly go over these technologies at this point. These techniques will be considered in more detail in the following chapters.

A.2.1. Semiconductor On Insulator (SOI)

One of these fundamental technologies necessary for realization of 3DI, is Semiconductor On Insulator technology[50-53]. Special techniques are needed to grow a crystalline semiconductor on top of insulators. This is due to the fact that many insulators have either amorphous structure, or that their lattice constant does not match the lattice constant of

the semiconductor. Furthermore, devices built on non-crystalline semiconductors (amorphous semiconductors) are inferior to those built on a crystalline semiconductor. Many applications require devices with a performance that exceeds the performance of devices built on amorphous semiconductors.

Origins of semiconductor On Insulator (SOI) technology, essential for realization of 3DI technology, dates back to early days of discovery of transistor[89]. Elleman and Wilman reported their efforts on growing PbS on NaCl in 1948[90]. In the 1950s, several efforts had been made to grow single-crystal Ge films on insulators[91-93]. The early incentives for these efforts was to avoid the increasing need for large single crystal wafers. Also, in the early days of semiconductor industry, there was a perception that the SOI technology was the best way to produce high resistivity materials for it utilized high resistivity materials for device isolation in a chip.[89] Work on Si based technology expanded in the late part of 1950s[89].

In the early days of Integrated Circuit technology, several advantages of SOI over single crystal wafer technology had been reported[89]. Device isolation was one of these benefits. The device isolation in this stage was achieved by back biasing a PN junction in the form of diffused guard rings. These isolation techniques were accompanied with the leakage current, specially for Ge based technology.

Another advantage of SOI technology is that the devices built on this type of substrate has less parasitic capacitance. This is due to the fact that only the side walls of a diffused regions on thin silicon film contributes to the capacitance; whereas, in a bulk silicon wafer, walls as well as the bottom of the diffused region make a contribution to the total capacitance. As a result of this reduction in parasitic capacitance, the device can achieve higher operating frequencies.

Since, there is less silicon for the generation of minority carriers, in case of a radiation exposure, SOI technology is more radiation resistant than bulk silicon material. Finally, some insulators have the advantage of having a higher thermal conductivity in compare to the bulk

semiconductors. This higher thermal conductivity improves the maximum power dissipation of a circuit, which is specially useful for miniaturization of the devices.

The advantages that SOI based technology enjoies in terms of speed, power dissipation, device isolation, and radiation resistance over the bulk silicon wafer technology provided the early incentives for research and developments on the Silicon-On-Insulator technology. Begining explorations were mainly focused on the structure shown in Fig. A.5a. These early efforts were concentrated on the deposition of a epitaxial grown semiconductor on insulating substrates such as calcium fluoride, quartz, sapphire, magnesium oxide, or the beryllium oxide[94].

Calcium fluoride, quartz and sapphire all have the same lattice constant as silicon, while the other three provide other advantages. For example, BeO has the advantage of having a higher thermal conductivity, which in turn improves the maximum power dissipation of a circuit. Even though, efforts in growing epitaxial silicon over BeO were reported by a handful of researchers in 1965[95]; further research in this area virtually came to an end as difficulties arose in obtaining large BeO crystals and more encouraging news in other areas were published[94].

MgO and CaF_2 react with the gases used in the epitaxial growth process; moreover, it is proven to be very difficult to produce single crystal silicon on top of these materials[96-97]. In addition, CaF_2 have a poor adherence of film to substrate[94].

Efforts on epitaxial deposition of Si on a single crystal quartz have been reported by Joyce et al[98]. Even though, single crystal islands were obtained for Silicon-Quartz structure; very large number of defects and extremely low carrier mobilities were observed on those islands[99-100]. Moreover, quartz substrates go through phase transition around 570 ^{o}C, which make it susceptible to fracture[94].

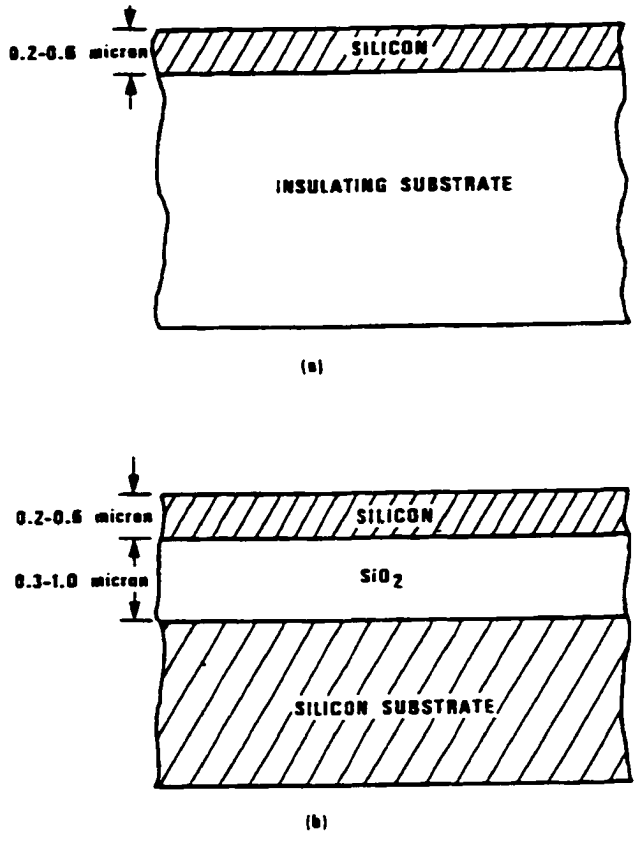


Fig. A.5. Silicon On Insulator structures (a) Substrate is from insulating material (b) Substrate is a silicon that is covered with thin insulator film , which in turn is covered with thin silicon film[101].

Studies involving deposition of Silicon On Sapphire and Silicon On Spinel were very rewarding. The first single crystal silicon on sapphire was reported in 1963 by Manasevit and Simpson[102]. Shortly thereafter attempts in growing epitaxial silicon on spinel were reported [103-104]. Silicon on sapphire was emerging as the most promising technology for SOI; even though, the interest in spinel was motivated by poor quality of early sapphire substrates, which was produced by the flame fusion technique. Moreover, P-channel MOS technology, which prefers (111) oriented silicon films of spinel, was the main subject of interest in those

early stages of IC technology[94]. However, with the shift of industry to n-channel MOSFET, which prefers (100) oriented silicon films, and the fact that (100) oriented silicon films grown on top of spinel had poorer mobility (in compare to similar silicon films grown on sapphire) the silicon on sapphire emerged as the major SOI technology[94]. Many researchers, including Manasevit[105], Filby and Nielsen[106], Cullen[107] , and once again Manasvit[108] have documented and reviewed this stage in development of SOI technology from historical perspective.

Recent interest in SOI technology has been mainly concerntrated with the second type of SOI structure, which is shown in Fig. A.5b. One of the incentives for the interest on this structure has been generated as result of 3DI technology's need for stacking many layers of plainly integrated circuit on top of each other. Due to another constrain of 3DI technology, which requires low temperature processing, poly-silicon or even amorphous material is deposited on top of a substrate first. These materials have very large defect density, which results in very low electron mobilities. Therefore, in order to improve the characteristics of these materials, several additional steps should be taken to improve their electrical characteristics. These steps, which include laser re-crystallization or electron beam re-crystallization, will be discussed later.

A.2.2. Chemical Vapor Deposition (CVD)

Chemical Vapor Deposition (CVD) can be utilized to produce this second type of SOI structure. CVD can be employed to deposit silicon and various other compounds on top of a great variety of substrates. Versatility of this powerful method for deposition of various materials is shown in Table A.4.[109]

Table A.4. Some important material deposited by CVD method[110].

Insulators	SiO_2, Al_2O_3, TiO_2, Ta_2O_5, Fe_2O_3, Si_3N_4, $Si_xN_yH_z$, BN, $Si_xO_yN_z$, $Al_xO_yN_z$
Semiconductors	Ge, Si (in all there forms, amorphous polycrystalline, signal-crystal) III-V semiconductors: GaAs, GaP, AlN, AlP, AlAs, GaN, GaSb, InP, InP, InAs, AlGaAs, GaAsSb, GaInP, GaInAs, InAsP, GaInAsP. II-VI semiconductors: ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe
Conductors	Metals: W, Mo, Al, Cr, Ni, Ta Silicides: WSi_2, $TiSi_2$, $TaSi_2$, $MoSi_2$, Doped-PolySilicon
Superconductors	Nb_3Sn, NbN, Nb_4N_5
Magnetic Materials	Ga: YIG, GdIG

Most these materials can be deposited at relatively low temperatures. For example, Aluminum could be deposited using this method at around 200°-300°C[111]. This feature of CVD is particularly useful for 3DI technology because high temperatures would result in diffusion of the impurities in the lower layers. Such a diffusion of impurities in lower layers, as it has been mentioned before, would result in the malfunctioning or destruction of semiconductor devices built on the lower layers. Moreover, a low temperature process minimizes the possibility of the process induced by crystallographic damage and wafer warpage. Further more, CVD technology make it possible to create both homogeneous and graded structures with excellent control in the composition of deposited materials[109]. Needless to say, these features could prove to be very valuable in fabrication of advanced microelectronic devices.

CVD technology has been utilized to produce unusual solid solutions and alloys, which can not be obtained by any other method[112]. This is partially due to the fact that in CVD technology, both the chemical composition and physical structure of deposited material can be

engineered, i.e., by tailoring the chemistry of the reactions and changing the deposition conditions of the material involved.

As one might expect from the name of this process, the components of a gas or vapor phase react chemically with the surface of the substrate to form a solid product. The final result is a thin film or thick coating of deposited materials. The deposited materials can be in any form: single crystalline, polycrystalline, or amorphous structure. The final structural form, in which the material is deposited, is determined by chemical agents and physical conditions present during deposition. Therefore, it becomes necessary to understand the physical conditions and chemical mechanisms involved in this process first; then using the knowledge gained, an attempt should be made to design proper devices to control the process.

One should be fully aware of the fact that CVD is different from the other physical deposition processes such as evaporation, sputtering, or MBE. This is due to the fact that there is always at least one chemical reaction involved in a CVD process; whereas, in other physical deposition techniques, no chemical reaction takes place. Therefore, understanding the real nature of a CVD process requires a good background in many areas of chemistry (including gas phase reactions, chemistry of free radicals, radiation chemistry, catalysis, and surface controlled reaction). In addition to considering all these areas in chemistry, one should not underestimate the importance of the physical conditions under which these chemical reactions are carried out in a CVD process. The physical conditions present in the time of deposition have a profound effect on the characteristics of a deposited film . Therefore, physical aspects of a CVD process, such as over all thermodynamics of the process, Kinetics of the gases involved, fluid mechanical consideration of the CVD reactor itself, heat transfer and it's associated problems in this process, possibility of the creation and the proper use of plasma, transport mechanism of the reactants and the byproducts, and physical considerations of film growth phenomenon should be fully studied. Here in this paper, no attempt has been made to fully cover all these aspects. A full study of all aspects of CVD process requires many

volumes. Nevertheless, a brief overview of some of the more important features of this technology, which relates to the subject in hand, follows. More detailed information regarding these process might be found in the references used for preparation of this review[109,113-141].

CVD reactions could be classified as homogeneous, heterogeneous, or a mixture of both. Heterogeneous and homogeneous reactions are defined as follows:[109] If gasses involved in the reaction nucleate while they are in the gas phase and produce particle, the reaction is called homogeneous. However, if these gasses or vapors react with the surface of substrate and produce particles which keep the crystal structure of the substrate, then the reaction is heterogeneous. Obviously, a heterogeneous reaction is preferable to a homogeneous reactions in most applications. For example, it is more desirable to deposit crystalline silicon than an amorphous silicon film.

A typical chemical reaction of a CVD process may include several steps, such as pyrolysis (thermally induced decomposition), synthesis, oxidation, reduction, hydrolysis, nitrite and carbide formation, disproportionation, and chemical transport.[142] One example for each type of reaction is presented in Table A.5.[143] Usually, an ordered sequence of a few of these reaction types is required to produce a specific end product. Controlling each step of a CVD process is possible by variation of variables involved in that step, such as temperature, pressure, amount and quality of a catalyst, concentration of the agents involved in the reaction, and elimination mechanisms for byproducts.

The energy required for the chemical reactions, involved in a CVD process, could be supplied by thermal heating, plasma, or electromagnetic radiation, which is usually in the form of ultraviolet or laser radiation. Higher temperatures in a CVD process generally lead to higher rate of deposition, higher density, and better structural crystallinity of deposited materials. Nevertheless, in an exothermic reaction, which is a reaction that produces heat, the substrate's temperature is kept below the temperature of other reactants involved in the process. This

method produces a yeild increase in an exotermic reaction. One should expect to do the reverse for endothermic reactions in order to increase the yield of the reaction. That is, in an endothermic reaction the temperature of the substrate is kept above the temperature of the reactants.

Table A.5. Examples for some of the processes involved in a typical CVD process.[143]

Pyrolysis	SiH_4 (g) -> Si (s) + $2H_2$ (g)
Reduction	WF_6 (g) + $3H_2$ (g) -> W (s) +6HF (g)
Oxidation	SiH_4 (g) + $4N_2O$ (g) -> SiO_2 (s) + $4N_2$ (g)+ $2H_2O$ (g)
Hydrolysis	$2AlCl_3$ (g) + $3CO_2$ (g) + $3H_2$ (g) -> Al_2O_3 (s) + 6HCl (g)+ 3CO (g)
Nitrite Formation	$3SiH_4$ (g) + $4NH_3$ (g) -> Si_3N_4 (s) + 12 H_2 (g)
Carbide Formation	$TiCl_4$ (g)+ CH_4 (g) -> TiC (s) + 4HCl (g)
Disproportionation	$2GeI_2$ (g) -> Ge (s) + GeI_4 (g)
Organometalic Reactions	$(CH_3)_3Ga$ (g) + AsH_3 (g) -> GaAs (s) +$3CH_4$ (g)
Chemical Transport Reactions	6GaAs (s) + 6HCl (g) -> As_4 (g) + As_2 (g) + GaCl (g) + $3H_2$ (g)

It is possible to predict the feasibility and efficiency of a reaction for given temperature and pressure analytically using the laws thermodynamics[144]; nevertheless, an accurate thermochemical data bank for values of free energies (ΔG_f^o), and enthalpies of formation (ΔH_f^o) for all the agents in the reaction is required. Moreover, one should note that these calculations could be made only for a reaction under thermodynamical equilibrium . Of course, chemical reactions of a CVD process are rarely at thermodynamical equilibrium state.

However, these calculations could serve as a first estimate for predicting the feasibility of the process.

These thermodynamical calculations for CVD reactions are indeed very simple, if one has access to a reliable database of the constants involved in the reactions. First, one should look up the chemical formation energies (ΔG_f^o) of each agent in the reaction. Then the reaction energy could be calculated by:

$$\Delta G_r^o = \underset{\text{All products}}{\Sigma \Delta G_f^o} - \underset{\text{All reactants}}{\Sigma \Delta G_f^o} \quad \text{Eq. A.1.1}$$

On the other hand constant of equilibrium (K_P) is given by[144]:

$$K_P \sim \frac{\underset{\text{All Products}}{\prod P_i^{a_i}}}{\underset{\text{All Reactents}}{\prod P_j^{a_j}}} \quad \text{Eq. A.1.2}$$

for a typical reaction of CVD, which could be written as:

$$a_1A\,(g) + a_2B\,(g) + a_3C\,(g) \ldots\ \Leftrightarrow\ b_1M\,(s) + b_2N\,(g) + b_3O\,(g) \ldots\ \quad \text{Eq. A.1.3}$$

where P is the pressure of each compound in the reaction, and a_i, b_j are the coefficient of that particular term. Moreover, it should be noted that there should be only one compound in solid form existing in this type of reaction: the deposited film. Other compounds in the reaction should be in form of gas or vapor in order to be eliminated from the reaction zone. Furthermore, the equilibrium constant (Kp) is related to the reaction energy as[144]:

$$K_P = e^{\left(\frac{-\Delta G_r^o}{2.3KT}\right)} \quad \text{Eq. A.1.4}$$

Therefore, by using Von't Hoff equation, one could find the enthalpy ΔH[144]:

$$\Delta H = RT^2 \frac{\partial K}{\partial T} \quad \boxed{\text{Eq. A.1.5}}$$

where T is the absolute temperature °K. Now, if ΔH turns out to be a negative value, this process is exothermic, i.e., produces heat. However, positive ΔH means that this process is endothermic , i.e., it consumes energy.

However, as it has been mentioned before, these calculations assume total equilibrium condition. In a real CVD reactor, chemical kinetics of the materials involved influence the overall process. Thus, the rate of deposition could be greatly influenced by factors such as: crystallographic orientation of the substrate, it's chemical composition, the surface site's density and geometry, and other physical features of the substrate's surface. The steps involved in kinetics of a heterogeneous CVD reaction could be classified as[125]:

1. Mass transport of reactant(s) to substrate
2. Adsorption of reactant(s) on substrate surface.
3. Chemical reaction (including surface diffusion) on surface.
4. Desorption of product gas(es) from surface.
5. Mass transport of product gas(es) away from substrate.[145]

The slowest step acts a bottle neck for the entire process, so it controls the overall rate of reaction. For example, if the third step is the slowest of all the steps, overall process has to wait for this step to be completed. Further more, the speed of each step is related to the temperature. In the low end of temperature scale the surface processes (steps 2,3, and 4) have the slowest reaction speed; therefore, they control the overall reaction rate. As a result this

type of process is called "surface limited". In a surface limited process the dependence of reaction rate to temperature change is very large due to rapidly increasing surface states with the increase in temperature. On the other hand, at the high end of temperature scale steps one and five are slowing the overall process. The chemical reactions under these types of conditions are called "diffusion controlled" processes. One important characteristic of this type of process is a weak dependence to temperature when compared to surface controlled reactions. This fact could be observed in Fig. A.6. In this figure, the deposition rate vs. temperature has been platted for several gases, which normally are used for silicon deposition in a CVD process.[145] It can be observed from this graph that different mechanisms are in control for different regions of temperature range.

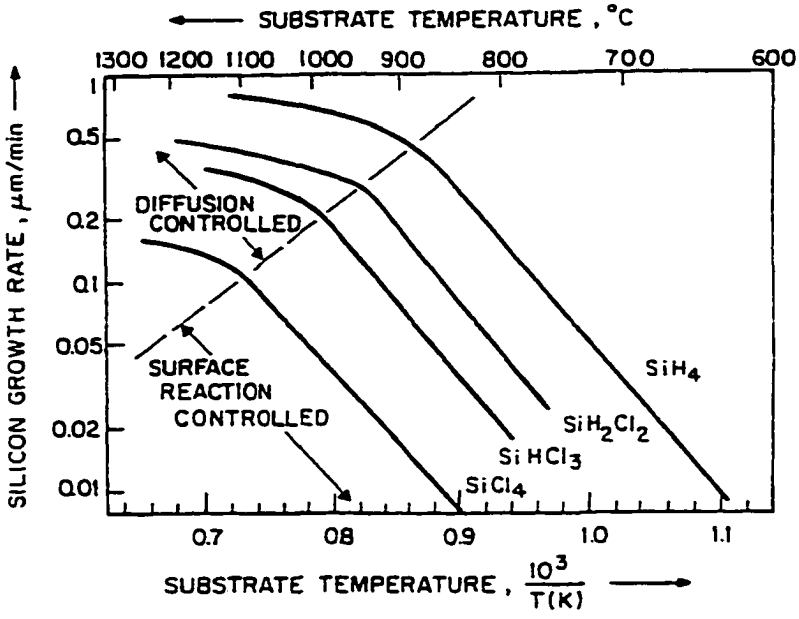


Fig. A.6 Deposition rate of Si vs. Temp. for various source gases[145]

Another important issue in CVD process is the transport phenomenon. Transport phenomenon of CVD covers areas, such as transfer of mass, energy, heat, and momentum to and from the substrate. Therefore a good understanding of this area is essential for controlling the process. These factors could influence the reactant access to the substrate. Moreover, these factors influence the temperature of the reactants, the elimination speed of the by-products from reaction zone, and transport of impurities inside the substrate. In a conventional CVD process, for example, convection, conduction, and radiation can each contribute to the heat flux. Convection's contribution stems from the flow of the gases; whereas, conduction's contribution depends on the type of gasses being used and their partial pressures. That is some materials are better heat conductors than the others. For example, H_2 and He are much better heat conductors than say N_2 or Ar. On the other hand, the flow of gases in the reactor, which directly related to heat convection, is effected by many factors such as: velocity of flow, pressure, system geometry, temperature and other physical properties of the gases and the vapors present in a CVD reactor. Finally, the contribution of the radiation should be taken into the consideration for temperatures above 400°C[146].

Another very important aspect of film growth, in a CVD technology, is nucleation and structural formation (i.e., crystalline, poly crystalline, or amorphous). As it has been mentioned before, the structural construction of the material determines, to a large extent, other physical properties of deposited materials such as: conductivity, electron mobility, and so on. Usually, to deposit materials with good quality high temperatures are needed.

A.2.2.1. Various Forms of CVD

There are many CVD technologies are available today. One way to classify CVD technologies is according to the way energy is supplied to the process. Currently, there are three major methods of supplying energy to the CVD process. One of the most popular methods of supplying energy to a CVD process is through thermal activation. That is, by

heating the gases and / or the substrates, the electron bonds in-between the reactants are broken and more surface sites become available for reaction. This process can be performed at different pressure ranges. The thermal energy could be supplied to the process by various methods, including: resistance heating, infrared radiation, microwave, or RF induction heating[118-119,146-150].

The second method of supplying energy to a CVD process is through plasma.[151-164] In this case, a RF or DC induced discharge glow is used to initiate and enhance the process. This type of supplying energy to a CVD process is usually done for cases where low temperature processing is important; therefore, this paper suggests that this method of CVD process to be used for deposition of materials by in 3DI technology. This issue will be addressed in more detail later.

Finally, a third way of supplying the energy to a CVD process is by using photons, electromagnetic radiation, with a very short wave length (ultra violate radiation). The photon energy could break the molecule apart and create the radicals necessary for the start of a reaction. This photons are absorbed by the electrons, which are holding the molecules together. The energy required for an electron, which holds two part of molecules together, to break free from its state can be supplied by a photon with energy E = hf. This leaves two radical ready for reaction. Due to quantum mechanical nature of this reaction, a photon should have at least an energy equal to or grater than the bonding energy. This means that in order to be effective the wave length of the light used should be shorter than $\lambda = \frac{hc}{E}$, where E is the bonding energy[165-170]. Here let us review specific examples for each case.

A.2.2.1.1 Atmospheric Pressure Chemical Vapor Deposition (APCVD)

Atmospheric Pressure Chemical Vapor Deposition (APCVD)[118,119], and Low Pressure Chemical Vapor Deposition (LPCVD)[146-150] are the two main types of thermally

activated CVD processes. In the APCVD, the reaction chamber (called "reactor") is kept slightly above normal atmospheric pressure. In order to achieve good uniformity for the deposited film, the pressure inside the reactor should be controlled. To control this pressure, the size of the exhaust opining is adjusted. The rate of film deposition in this type of CVD is controlled by the temperature and the reactors rate of flow. Similar to other thermally activated CVD processes, in APCVD heat is supplied by means of resistance heating, RF heating, or infrared radiations.

The only advantage of this type of CVD over other types is the simplicity of the procedure. No vacuum pumps or other sophisticated equipments are needed; therefore, less capital is needed to setup such a process in comparison to other types of CVD processes. Two main disadvantages of these processes are the high temperature requirement to produce good quality deposited films and the homogeneous nucleation, which might contaminate the deposited film. As mentioned before, in a homogeneous nucleation reaction gases or the reactants nucleate while they are still in the gas or vapor phase. These particles precipitate everywhere, including the walls of the reactor. The particles precipitated from the previous processes on the walls of the reactor may react with the gases and reactants of another process and produce contamination for the CVD process. Special techniques are used to remove such unwanted particles from the walls of the reactor.

A.2.2.1.2. Low Pressure Chemical Vapor Deposition (LPCVD)

Low Pressure Chemical Vapor Deposition (LPCVD) is very similar to APCVD. The only difference is the pressure range in which this process is performed.[116-150] When the gas pressure is lowered, the effect of the mass transfer rate increases in comparison to the surface reaction rate, making it possible to deposit highly uniform films in a closely spaced substrates placement. Therefore, the overall process become highly economical. Today, this process,

LPCVD, is one of the most cost efficient technologies utilized in semiconductor industry to deposit various materials including, insulators, amorphous and polycrystalline silicon, silicides, and refractory metals.

LPCVD's process mechanism could be explained as follows:[146] The thinner the slowly moving gas layer adjacent to the substrate , the higher the diffusion rate of the gas and the greater the mass transfer from the gas to a substrate. On the other hand, a surface reaction rate mainly depends on the reactants' concentration and the deposition temperature. The diffusitivity, D, and boundary layer thickness, σ, are given as:[171]

$$D = \frac{C_1 T^{\frac{3}{2}}}{P\sigma^2 M^{\frac{1}{2}}} \qquad \text{Eq. A.1.6}$$

and

$$\sigma = C_2 \left[\frac{XV\rho}{\mu}\right]^{\frac{-1}{2}} - C_3 \qquad \text{Eq. A.1.7}$$

in which, C_1, C_2, C_3 are constants. T is the absolute temperature, σ is the collision diameter, M is the molecular weight, X is the distance from the leading edge of the boundary layer, V is the free velocity of the stream, and μ is the viscosity of the fluid. Table A.6 is briefly compares the characteristics of LPCVD process performed at 0.76 Torr (0.001 Atm.) with an APCVD process performed at 760 Torr (1 Atm.).[171]

As it can be observed from this table, the diffusitivity of LPCVD is 1000 times greater than APCVD; however, LPCVD has a 3 to 10 times thicker boundary layer (σ). Such a small change in the boundary layer thickness does not offset the huge diffusitivity advantage of LPCVD over APCVD. Therefore, lower pressures in CVD process greatly enhance the mass

transfer rate, making it possible to closely place substrates. This creates a huge economical advantage for mass production. Moreover, the unusually high deposition rates achieved with LPCVD are credited to the fact that relative mole fraction of the reactant gases is large in comparison to APCVD. This is mainly as result of using little or no diluent gases in this process.

Table A.6. A comparison between LPCVD and APCVD[146,171].

Gas Parameter	LPCVD	APCVD
Pressure, P	1	1000
Diffusitivity, D	1000	1
Velocity, V	10-100	1
Density, ρ	1	1000
Reynolds Number, RE	1	10-1000
Boundary Layer Thickness, σ	3-10	1

Wafer spacing is an important factor in LPCVD. For example, the deposition rate of this process increases linearly with increased spacing; this is because more reactant is available for each wafer. Other crucial factors in LPCVD, which could effect the thickness uniformity, are the pressure, the temperature profile, and the flow rates. In order to achieve uniform thickness on each substrate, these variables might be adjusted. For instance, in a tubular reactor, by increasing the temperature or the pressure, one might increase the deposition rate upstream of the flow.[171] This comes as result of thaving more reactant gases that would be consumed closer to the input valve, leaving less reactant gases for further away parts. Of course, one should expect the opposite effect by lowering the temperature or the pressure.

Similarly, one might affect the deposition uniformity by changing the rate of gas flow at a constant partial pressure, or the size and the number of wafers, which are produced per run. The main advantages of LPCVD could be summarized as follows:

- Substantially improved uniformity of the deposited films in compare to APCVD deposited films, due to better control of factors mentioned above.

- Fewer defects in the deposited films due to much lower particle contaminations and pinholes as a direct result of cleaner hot wall processes, such as LPCVD.

- Vertical positioning of the wafers that not only brings the costs down for mass production of the units, but also reduces the chance of co-deposition of homogeneously nucleated materials.

Off course, the argument could be made that the greatest disadvantage of LPCVD over APCVD is its requirement for more complex equipments, such as complex vacuum pumps. Therefore, higher costs of accusation, maintenance, and repair are more for LPCVD than they are for APCVD.

A.2.2.1.3. Plasma Assisted Chemical Vapor Deposition (PACVD)

Some researchers have taken LPCVD one step further, utilizing the properties of a glow discharge plasma where highly reactive agents could be created towards the goals of a CVD process.[151-164] This particular version of CVD process is known as Plasma Enhanced Chemical Vapor deposition (PECVD), or Plasma Assisted Chemical Vapor Deposition (PACVD).

The plasma itself is usually created at pressures ranging from 0.01 to 1 Torr by application of an electric field on the gas molecules. This electric field breaks down the gases'

molecules into very reactive radicals. The form of this electric field could be RF, AC, DC, or even microwave, which is generated by a RF, AC, DC, or microwave sources, respectively.

One should be advised to the non-equilibrium nature of plasma. That is, the reactants themselves might be at ambient temperatures, while their electron's effective temperature could be one or two orders of magnitude higher. Therefore, one should expect the chemical reactivity of these molecules, which have low temperatures themselves, to be almost as high as their normal reactivity when their overall temperature is equal to their electron temperature, since the electrons are mainly responsible for a chemical reaction. Consequently, using this technique, high temperature chemical reactions could be made to take place at lower temperatures. This feature of PECVD is extremely useful for the 3DI technology, since high temperatures could ruin the previously built layers. Moreover, low temperatures make the overall process more efficient.

Many variables can effect the deposition rate and other features of deposited film in a PECVD process:

- The power density of the electric field.
- The distribution of the electric field's power density over the reaction zone.
- The composition of the gases involved.
- The distribution of the gases inside the reactor.
- Temperature and its distribution inside the reactor.
- Total pressure in the reactor.

Major features that could be effected by these variables are the thickness uniformity and the crystalline structure of the deposited materials. Among the variables mentioned above, which effect the deposition rate and other features of the deposited materials in a PECVD process,

particular attention should be given to the distribution of electric field power density over the reaction zone. This is mainly due to the fact that the life time of plasma generated and highly reactive species is very short. Therefore, they should be generated very close to the desired reaction zone.

A majority of the PECVD processes are performed at the temperatures ranging from 250°C to 400°C under the overall pressure of 0.1 to 2 Torr.[172] Currently, this method is very popular for depositing "inter-aluminum insulating layers in multilevel VLSI silicon circuit, secondary Passivition films of plasma silicon nitrite on semiconductor devices, and hydrogenated amorphous silicon layer for thin film solar cells"[172]. Due to generation of the free radicals by electric field, this technique has a much higher rate for film deposition than LPCVD or APCVD. In addition, the overall deposited film has better features.

An argument has been made in regard to the disadvantages of PECVD when compared with other types of CVD processes.[151] This argument states that the overall complexity of the process and the reactions involved "makes the synthesis of Stoichiometric composition difficult"[9]. Furthermore this view points out that as a result of low temperatures (usually used in this type of CVD for deposition of the materials) gas molecules can become trapped inside the film. Another problem associated with Plasma Enhanced CVD is the radiation damage to the devices (such as MOS), which has been already built on the substrate. Most of the complications associated with radiation damage caused by Plasma Enhanced CVD can be eliminated by a thermal annealing after the deposition.

Recently, a new method for creation of plasma for PECVD has been introduced[173,174]. This new method allows one to deposit the films at very low temperatures with high deposition rates. In this process the plasma is produced by resonance of microwave radiations and electrons through a microwave discharge process in presence of a strong magnetic field[172]. This means an Electron Cyclotron Resonance (ECR) source of ion is employed to generate the high density plasma needed for this process.[172-174] The high

deposition rate that could be achieved at low temperatures in this procedure might prove to be very useful for 3DI technology.

A.2.2.1.4. Photon-Enhanced Chemical Vapor Deposition (PHCVD)

Let us review a recently introduced version of CVD process before reviewing a few specific examples of depositing key materials by CVD processes that can be adopted for 3DI technology. This method of CVD processes is called PHoto-enhanced Chemical Vapor Deposition or PHCVD. PHCVD utilizes very short wave electromagnetic radiation to release the bonding electron in a chemical compound (these radiations are usually in the range of short ultra-violate part of spectrum). As a result, highly reactive radicals are generated.[165-170] These radicals react with the surface of the substrate to produce deposits of the desired film.

Usually, mercury vapor is mixed with the gases in the reactor to act as photosensitizer. The molecules of the mercury vapor, having been mixed with the gases inside the reactor, become excited by a very high intensity quartz mercury resonance lamp with a radiation wave length of 253.7 nm. Next, these excited species collide with the other molecules in the reactor and transfer their energy to them. This generates free radicals and initiates the CVD process. This process continues as long as the mixture of the gases is exposed to the light source.

This promising and versatile version of CVD can offer several advantages over other types of CVD processes for 3DI technology. The most important advantages of this process is the low temperature requirement for film deposition. Most materials can be deposited with the help of this technology at around 150°C. There has been a number of reports indicating that most key materialsin the area of IC fabrication has been deposited at this temperature using PHCVD technology, including SiO_2[166,167,170], Si_3N_4[165,169] and Silicon[168]. It has been noted that the radiation damage in PHCVD is significantly less than the radiation damage caused by PECVD.[175]

At this point, let us consider some of the problems facing this technology. One of the first barriers that PHCVD technology needs to overcome is the unavailability of economically sound and commercially available production equipments. The need to use mercury vapor in order to achieve reasonable rates of deposition may pose another problem. This is due to the fact that mercury atoms could act as an impurity in the deposited film; therefore, the effect of this impurity should be fully taken into the account in designing a process. Moreover, current research concentrates on photolysis without the introduction of mercury. There has been some achievement in this area by utilizing very intense radiation of a high energy photon in the far end of ultraviolet range of the spectrum.[174]

A.2.2.2. Depositing Key Materials at Low Temperatures Using CVD Process

Here, let us briefly review the most common procedures and conditions under which some of the key materials are deposited on the substrate. Since insulating materials have a wild spread applications, it will be considered first. Next the deposition of semiconductors will be reviewed in some detail. In the final part of this section, deposition of metals, metal alloys, and silicides will be presented.

A.2.2.2.1. Deposition of Insulators

Today, insulating materials that have been deposited by various forms of CVD technologies function as capacitor's dielectrics, protective coatings, thinox, field oxides, inter-metal insulators, and so on.[146,176-177] Some of the chemical reactions used for producing insulators are listed in Table A.7.[178]

Even though, there are several reactions that could be adopted by a CVD procedure to deposit SiO_2 on a substrate; the most common way of depositing SiO_2 films on a substrate is by reaction of silane (SiH_4) and oxygen (O_2), which have been diluted in N_2, at about 300-450°C. This material, SiO_2, can be deposited at lower temperatures of about 250 to 350°C by

PECVD process.[151-154,156,158-164, 178-183] This technique is currently utilized to deposit an insulating film in-between two layers of metal in multilevel VLSI structures. The reaction involved in this type of CVD is as follows:[184]

$$SiH_4 + 2N_2O \xrightarrow[250\text{-}350^oC]{0.5\text{-}2\ Torr.} SiO_2 + 2N_2 + 2H_2 \qquad \text{Eq. A.1.8}$$

Since low temperature processing is very essential for 3DI technology, this last process might be utilized for depositing all the oxide layers in this technology.

Table A.7. CVD reactions to produce insulator materials.[178]

Product	Reaction
SiO_2	$SiH_4 + O_2 \xrightarrow[300\text{-}500^oC]{N_2\ \&\ Ar} SiO_2 + 2H_2$
SiO_2	$Si(OC_2H_5)_4 \xrightarrow[740^oC]{N_2\ \&\ Ar} SiO_2 + 2H_2O + 4C_2H_4$
SiO_2	$SiX_4 + 2H_2 + 2CO_2 \xrightarrow[1200^oC]{H_2} SiO_2 + 4HX + 2CO$
$Si_xN_yH_z$	$3SiH_4 + 2N_2 \xrightarrow[250\text{-}500^oC]{N_2\ \&\ plasma\ \&\ 0.5\ Torr} Si_xN_yH_z + xH_2$
Si_3N_4	$3SiH_4 + 4NH_3 \xrightarrow[750\text{-}1000^oC]{NH_3\ \&\ H_2} Si_3N_4 + 24H_2$
Si_3N_4	$3SiCl_4 + 4NH_3 \xrightarrow[750\text{-}1100^oC]{NH_3\ \&\ H_2} Si_3N_4 + 12HCl$
Al_2O_3	$2Al(OC_3H_7)_3 \xrightarrow[420^oC]{N_2\ \&\ O_2} Al_2O_3 + H_2O + C_xH_y$
Al_2O_3	$Al_2Cl_6 + 3CO_2 + 3H_2 \xleftrightarrow[900\text{-}1200^oC]{H_2} Al_2O_3 + 6HCl + 3CO$
$(SiO_2)_{1-x}(P_2O_5)_x$	$(1\text{-}2x)SiH_4 + 2xPH_3 + 3[O_2] \xrightarrow[300\text{-}500^oC]{N_2\ \&\ O_2} (SiO_2)_{1-x}(P_2O_5)_x + [H_2]$
$(SiO_2)_{1-x}(B_2O_3)_x$	$(1\text{-}x)SiH_4 + xB_2H_6 + 2[O_2] \xrightarrow[300\text{-}500^oC]{N_2\ \&\ O_2} (SiO_2)_{1-x}(B_2O_3)_x + [H_2]$

Similarly, to deposit nitrite (which acts as impurity barrier) and oxynitride of silicon (which usually functions as insulator) APCVD or LPCVD procedures are most commonly used. Si_3N_4 is usually produced from NH_3 diluted silane, or from diluted $SiCl_4$ in NH_3.[118,146-147,185] These reactions could be carried out at temperatures ranging from 800 to 900°C by APCVD or LPCVD techniques. In order to produce Si_3N_4 at lower temperatures and finer quality, one might use the reaction of dichlorosilane and NH_3 in a LPCVD process. The reaction temperature is around 700-850°C.[186] To produce $Si_xN_yH_z$, on the other hand, one might utilize PECVD process and the reaction:[151-154, 156, 158-161, 163,176-177, 179-183, 187-190]

$$SiH_4 + NH_3 \xrightarrow[0.2\text{-}3\ \text{Torr.}]{250\text{-}500^oC} Si_xN_yH_z + H_2 \qquad \text{Eq. A.1.9}$$

As it can be seen in this reaction formula, the reaction temperature is around 250-500°C, making it very attractive to the low temperature processing requirement of 3DI technology.

A.2.2.2.2. Deposition of Semiconductor

Now, let us consider deposition of silicon, which is another key material in fabrication technology. Silicon may be deposited from many a large variety of materials through many different versions of CVD process. For example, silane (SiH_4), monochlorosilane ($SiClH_3$), dicholorosilane ($SiCl_2H_2$), tricholorosilane ($SiCl_3H$), or the tetracholorosilane ($SiCl_4$) all can be used in a CVD process for depositing silicon. The formula for some of these reactions is given below:[191]

$$SiH_4 \xrightarrow[200\text{-}300^oC]{H_2\ \&\ \text{plasma}\ \&\ 0.5\ \text{Torr}} 2H_2 + Si \ \text{(amorphous)} \qquad \text{Eq. A.1.10}$$

$$SiH_4 \xrightarrow[800\text{-}1000^oC]{H_2\ \&\ He} 2H_2 + Si \ \text{(heteroepitaxial)} \qquad \text{Eq. A.1.11}$$

$$SiCl_4 + 2H_2 \xleftrightarrow[1200^oC]{H_2} 4HCl + Si \ \text{(homoepitaxial)} \qquad \text{Eq. A.1.12}$$

$$SiCl_3H + H_2 \xleftrightarrow[1200^oC]{H_2} 3HCl + Si \text{ (epitaxial)} \quad \boxed{\text{Eq. A.1.13}}$$

As it could be noticed from these reactions, in order to deposit silicon at lowest temperatures possible, one has to use silane (SiH_4), which is relatively expensive in compare to other materials. Moreover, the deposited material is in amorphous form. It is well known that the amorphous silicon has an inferior electronic characteristics. On the other hand, the other reactions have very high temperatures, which are not suitable for 3DI technology. Polycrystalline silicon has electrical characteristics that are better than amorphous and worse than single crystalline silicon; however, it could be deposited at lower temperatures, which could meet the low temperature requirement of 3DI technology. To deposit polycrystalline silicon (polysilicon) , the same source material, SiH_4, can be used with the same basic reaction. However, the temperature of the reaction should be raised to a 600-800°C range and pressure should be dropped to 0.1 to 1 Torr range.[191] Most processes choose their operating temperature to be 625°C for this purpose. There have been some reports that suggest the material deposited with this method at 650°C temperature had a thickness uniformity of better than 5%, which is considered to be good. Further more, the report indicates that growth rates were 10 nm per minute.[191] Nevertheless, silane is not the only material used for deposition of a polysilicon layer; other materials such as dichlorosilane ($SiCl_2H_2$) might also be used for deposition polysilicon. The reaction for dichlorosilane is as follows:

$$SiCl_2H_2 + H_2 \longrightarrow Si + 2HCl + H_2 \quad \boxed{\text{Eq. A.1.14}}$$

It is possible to dope the polysilicon layer while it is being deposited. This is usually done by mixing B_2H_6, PH_3, or AsH_3 with the gases in the reactor along with the other gases required for deposition. However, one should note that the doping of the material being deposited usually changes the growth rate of the depositing film as well as the overall uniformity of the film.[191]

A.2.2.2.3. Deposition of Metal and Alloys

Last but not least, let us review the deposition technique of metals, metal alloys, and metal silicides. There are three major CVD processes commonly used for depositions of the metals:[118, 192-193]

1. Organometallic compounds' pyrolysis.

2. Metal compounds' reduction, the halides' especially.

3. The process of chemical transport.

Let us start with tungsten, which is one of the most common metals used in the semiconductor fabrication technology. Recently, this metal has gained special importance in multilevel VLSI technology, where it has been utilized as refectory conductor.[194-200] Moreover, tungsten's many desirable characteristics make it an ideal metal for self-aligned technology. It is also considered to be a good diffusion barrier and could function as gate metal in MOSFETs, MESFETs, and many other devices. In addition the Schottky barrier of this metal will be used in this paper for specially architectured devices, designed for 3DI technology. Even though, tungsten has greater resistivity than aluminum; its lower metal migration tendencies, higher temperature stability, higher resistance to corrosion, and closer resemblance of it's thermal expansion coefficient to silicon's usually makes it more desirable than aluminum. Nevertheless, aluminum is still being used for other purposes in the fabrication technology.

CVD of tungsten is normally achieved by one of these three methods:[201]

1. Non-selective reduction: H_2 reduces WF_6 at high temperatures.[196-198]

2. Selective reduction: H_2 reduces WF_6 at low temperatures.[192-200]

3. Selective displacement of W by Si in WF_6: WF_6 is reduced by substrate's Si to form SiF_4 in the gas form.[196,198-200]

The first method utilizes the well-known reaction of Hydrogen with metal halides to produce the desired metals, in this case tungsten:[196-198, 201]

$$WF_6 + 3H_2 \xrightarrow[1\ Torr.]{450\text{-}700^oC} W + 6HF\ (gas) \quad \boxed{\text{Eq. A.1.15}}$$

As it can be seen in the equation above, this reaction is performed at temperatures between 450 to 700°C under one Torr of pressure by a LPCVD process.

The second method uses the same reaction at at temperatures below 400°C. In such low temperatures, hydrogen that has been adsorbed on the insulator surfaces would not be able to go through catalytic dissociation to generate atomic hydrogen; however, it still could be dissociated on Si and tungsten. Therefore, this method is good for thickening the thin silicon films deposited with the other methods, including the next method which will be presented shortly.

One should note in these two methods tungsten is reduced by hydrogen and not by the silicon; therefore, no silicon of the substrate is consumed. Moreover, the only difference between the last two methods is the temperature. As a result, by increasing the temperature, WF_6, or the deposition timing tungsten might deposit everywhere on the substrate, losing the advantage of the selectivity in the second process.

The last method is based on the reduction of tungstenhexafloride (WF_6) by the substrate's silicon. The method is based on the following reaction:[201]

$$2WF_6 + 3Si \xrightarrow[0.64\ Torr.]{300^oC} 3SiF_4 + 2W \quad \boxed{\text{Eq. A.1.16}}$$

As it can be seen from the above formula, this reaction is performed by a LPCVD process at 300°C temperature and 0.64 Torr of the pressure. Several important facts about this reaction should also be noted. This reaction is highly sensitive to substrate surface cleanness,

the surface should have very few negative oxides.[201] A second fact about this reaction is that two volumes of silicon on substrate are consumed for each one volume of tungsten generated. This means that the substrate surface where this reaction has taken place goes lower than the rest of the substrate. Finally, it should be noted that this reaction is self limiting, that is only 10 to 15 nm of tungsten could be deposited by this method. If thicker layers of tungsten are required, the second method, which has been described above, could proceed this method for thickening the deposited tungsten layers.

Most other metals and metal alloys could be deposited by various form of the CVD processes; nevertheless, only Al and Mo are currently deposited for commercial purposes.[201] The deposition process for Mo is very similar to that of tungsten, since Mo is prepared from MoF_6. However, aluminum has completely different CVD deposition processes, due to problems associated with the aluminum.[202-203]

A.2.2.2.3.1. Deposition of Aluminum

There are a few processes available for deposition of aluminum. In one of the most promising ones, aluminum is deposited from tri-isobutyl aluminum ($[(CH_3)_2CH\text{-}CH_2]_3Al$), called TIBAL, by LPCVD process using following reactions:[204]

$$(CH_3)_2CH\text{-}CH_2]_3Al \xrightarrow{50\text{-}150^oC} [(CH_3)_2CH\text{-}CH_2]_2AlH + (CH_3)_2C{=}CH_2 \quad \text{Eq. A.1.17}$$

and then this reaction follows by a second reaction:[204]

$$[(CH_3)_2CH\text{-}CH_2]_2AlH \xrightarrow{220\text{-}330^oC} Al + \frac{3}{2} H_2 + 2(CH_3)C{=}CH_2 \quad \text{Eq. A.1.18}$$

This method of depositing aluminum has overcome most of the drawbacks of conventional techniques for depositing aluminum.[202-203] The advantages of this technique

are the its conformal coverage of the substrate, high wafer throughput, and production of surfaces with few surface states. Furthermore, it has been reported that this method of LPCVD for aluminum produces excellent adhesion to the substrate, very good chemical purity, low contact resistance, and high electrical conductivity. Nevertheless, two major problems remain in aluminum deposition technology. The first one deals with electromigration, and aluminum is especially notorious for this problem. The second problem is the aluminum silicon inter-diffusion. These problems could be reduced considerably by techniques, such as placement of a diffusion barrier in-between aluminum and the silicon.[203]

A.2.2.2.4. Deposition of Metal Silicide

In the last part of this discussion about CVD of conductors, let us briefly overview the CVD processes for deposition of metal silicides. Metal silicides are considered to be one of the most important replacements for metals in semiconductor industries. They have generally good adhesion to the silicon substrates, excellent conductivity, few interface states, favorable characteristics for dry etching, and good stability in high temperatures.[204-206] Some of the most import metal silicides currently used in semiconductor industry are: $TaSi_2$[207-208, 209] , WSi_2[195,210-211,209], $TiSi_2$[212, 209], and $MoSi_2$[213, 209].

Even though, these silicides can be prepared by E-Beam Evaporation, or Magnetron Sputtering[214]; LPCVD process is more advantageous in terms of step coverage, material purity, shrinkage, stress, and composition control of the deposited material.[209]

Among all the metal silicides, tungsten silicide (WSi_2) and titanium silicide ($TiSi_x$) have the most developed technology. Tungsten silicide is prepared at a 330-370°C temperature range under 50 to 300 mTorr of pressure by LPCVD technique. The chemical reaction for preparation of this material is shown below:[205-206, 210-211, 215]

$$WF_6 + 2SiH_4 \xrightarrow[300\ mTorr.]{330\text{-}370^oC} WSi_2 + 6HF + H_2 \quad \boxed{\text{Eq. A.1.19}}$$

and titanium silicide can be prepared at a 300 to 500°C temperature range by the PECVD process from the reaction of SiH_4 and $TiCl_4$.[206,210-213,215] There have been some reports indicating that bulk resistivity of 30 to 60 μΩ–cm for tungsten silicide (WSi_2) and 15 to 20 μΩ–cm for titanium silicide ($TiSi_x$) has been achieved.[205-206,210-213, 215] Incidentally, the bulk resistivity reported for $TiSi_x$ is the lowest of all reported bulk resistivities for any refractory metal silicides to the time this paper was being prepared.[215]

However, these are not the only metal silicides available; many other metals form metal silicide with silicon. Table A.8 categorizes the metals in terms of their ability to form metal silicides.[216] As shown in this table most metals in the lower left part of the periodic table can form metal silicide with silicon.

Table A.8. Periodic table of silicide formation.[216] All the metals form silicides except those written with a shadow font, such as Al.[217] Those metals that from silicide by solid-state thermal reaction at comparatively low temperatures are underlined, such as W.[218] Also, the rare earths Gd, Tb, Dy, Ho, and Er also form silicides by low-temperature solid state reaction.[216]

Li	Be													
Ka	Mg											Al		
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi

A more detailed discussion about metal silicides and their production techniques has been presented by Murarka[219].

A.2.3. Planarization Technology

Another important requirement for the development of 3DI technology is planarization technology. Due to the many steps of processing for each layer of integrated circuit, the substrate surface can become too uneven for successful completion of lengthy processing steps necessary for construction of subsequent layers, such as lithography. Fig. A.7 clearly demonstrates the requirement for some sort of planarization technique for 3DI technologies[220].

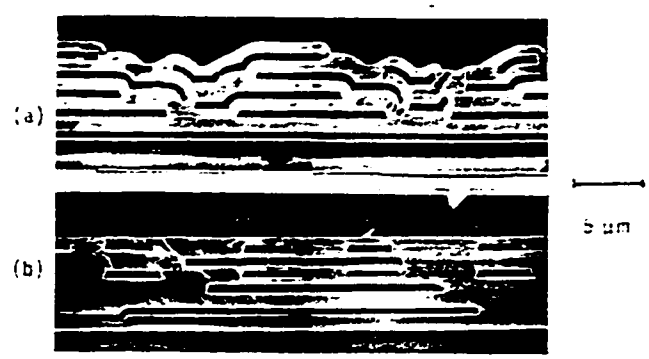


Fig. A.7. Cross section of a 5 layer substrate (a) without (b) with utilization of planarization technology.[220]

A wide range of planarization techniques have been developed in recent years; however, most of these techniques are not totally compatible with the requirements of 3DI technologies. Each technique offers its own unique advantages, which is packaged with the associated problems of that particular technique. Like many other engineering problems, compromise should be made before incorporating these techniques into a 3DI technology.

It would require several volumes to cover all the aspects of planarization techniques with reasonable detail; therefore, it is impossible to cover all the planarization technologies in this paper. Moreover, many of the planarization technologies available today are not compatible with the requirements of any 3DI technology . Nevertheless, a few of these techniques, which have great potential to be incorporated in a 3DI technology, will be introduced in this paper. One does acknowledge, however, that further developments should be made in some of these techniques to make them more compatible with 3DI requirement.

Before considering some of these planarization techniques, let's define planarization in a more scientific and mathematical language. In order to do this, let's consider Fig. A.8.[221] Planarization could be defined as the difference in the heights of a feature before and after the planarization process divided by the height of the same feature before planarization process. Therefore, the degree of planarization in Fig. A.8 could be written as:[221]

$$P = \frac{h_\mu - h_\rho}{h_\mu} \qquad \text{Eq. A.1.20}$$

As it could be seen from Fig. A.8 all the features of a substrate won't achieve the same degree of planarization for a given planarization process. This fact leads to the introduction of several concepts in planarization technology[221]. One of the concepts resulting from this fact is the regional or local planarization. Local planarization is a term that refers to quality of planarization over one or few devices. Usually in this type of planarization, the area of interest is limited only to few μm^2. Local planarization deals with the filling of holes on the substrate,

smoothing the raged edges of oxides, and so on. Another planarization concept deals with overall planarization of the substrate itself. This type of planarization interpretation is called global planarization. M. W. Horn has defined the boarder line between these two planarization concepts, for current state of technology, to be 10 μm^2.[221]

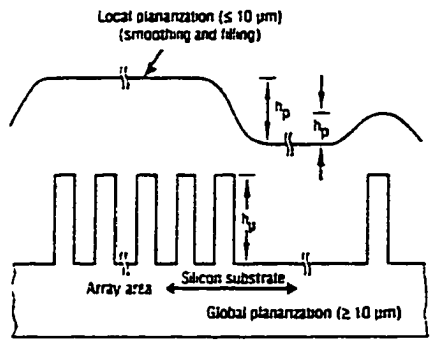


Fig. A.8. Global and local planarization.[221]

A few of the more popular planarization processes with better local planarization results are listed below:[221-228]

1. Thermal reflow.[222]

2. Deposition by bias Sputtering.[223]

3. Biased CVD.[224]

4. Biased PECVD, utilizing Electron Cyclotron Resonance (ECR).[225]

5. Spin on glass.[226]

6. Use of Polymers, especially Polyamide.[227]

7. Fusion Flow of BoroPhosphoSilicate Glass (BPSG).[228]

Similarly, Global planarization could be best achieved by Sacrificial Etchback (SE)[221, 229-230], or Chemical-Mechanical Polishing (CMP)[221, 231-236] methods. Let's take a closer look at a few of these techniques.

A.2.3.1. Spin On Layer Planarization Technique

Spin On Layer technique utilizes the principle that molten and viscous materials planarize a topography by their flow. The main forces that effect the flow of materials at low rotational speeds are the capillary force and the force of gravity; however, the force of gravity is negligible when compared to capillary forces for most coating materials. By applying the principles of fluid mechanics to the flow of a viscous material and ignoring the negligible effects of the force gravity, an equation could be driven to estimate the degree of planarization:[237]

$$P = F(x) = F\left(\frac{t\ \gamma\ h_o^3}{\eta\ w^4}\right) \qquad \text{Eq. A.1.21}$$

t = Time spent on the planarization process.

γ = Surface tension.

h_o= Initial film thickness.

η = Viscosity.

w = Width of feature being planarized.

The function F(x) in the above equation is a feature dependent function: its value is very close to zero for x<< 0.1 and very close to one for x>> 0.1. This function is monotonically increasing and has a sharp slop for values less than 0.01.[221] One might observe from the above equation that planarization is inversely related to fourth power of the width of the feature being planarized. As a result, the larger the width of the object the lesser the capillary force and the degree of planarization. Therefore, this method is better suited for local planarization than for global planarization. The empirical results also confirm this fact. Fig. A.9 clearly demonstrates that the degree of planarization decreases with an increase in width of the trench.[221]

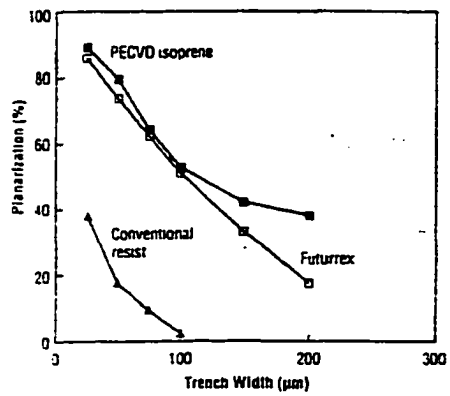


Fig. A.9. "Planarization vs. Trench width for 2 μm thick film of different organic layers (trench depth ~ 1.2 μm)"[221]

A.2.3.1.1. The Dependence of the Meterial Characteristics on Spin Coating Planarization

Two other variables that could be manipulated (by changing the material used for coating) are the film viscosity (η) and the surface tension (γ) between the substrate surface and

the coating material. Therefore, utilization of appropriate organic materials, such as polyamid, the surface tension will increase by a factor of 2 or 3.[227] Similarly, viscosity could also "vary by two orders of magnitude, depending on temperature, structure, molecular weight, and polydispersity"[238]. Obviously, the more time spent on the planarization process, the higher the degree of planarization that could be achieved. This fact could be concluded from the above formula as well. Fig. A.10 and Table A.9 present empirical data for the relationship between time spent and the degree of planarization.[239]

Table A.9. "Percent Planarization Versus Leveling Time for Epoxy A Film"[239]

Leveling Time (Sec)	Planarization (%) For gap width:		
	75μm	250μm	1000μm
0	2	2	1
15	53	19	11
30	73	26	22
60	85	37	36
120	88	50	50
600	95	72	70

It should be noted that several assumptions have been made in driving the last equation.[237] For example, an assumption was made that the liquid is a viscous and a Newtonian liquid. However in most cases, the organic materials used for coatings are not Newtonian. Both the viscosity and the surface tension of these liquids is a function of time and temperature.[221] Therefore, the optimum leveling time should be determined by experimental means. Nevertheless, the results of this formula could be used as a first approximation.

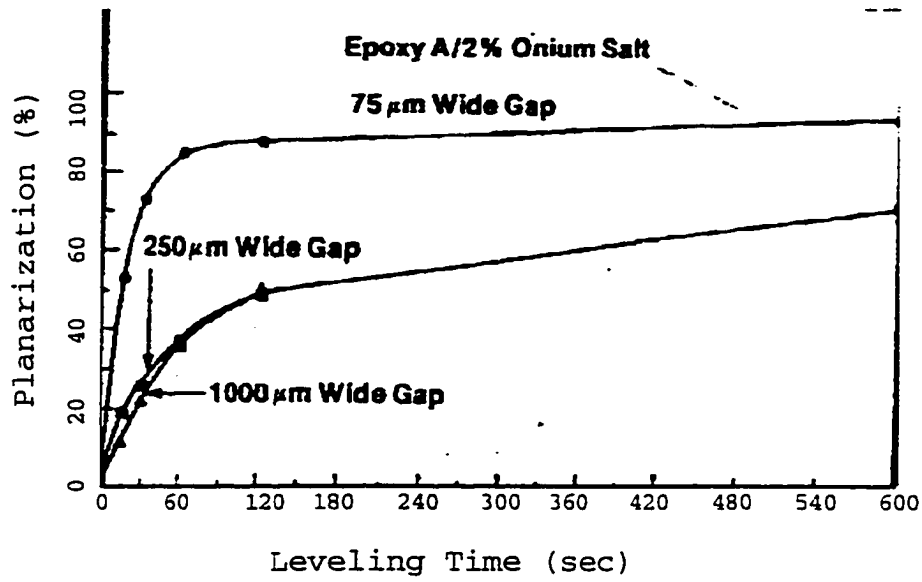


Fig. A.10. Planarization plot of the 75, 250, 1000 μm gap widths vs. time for epoxy A films.[239]

Another assumption in driving the previous equation was that the main propelling force of this planarization process was the capillary force.[221] This is the case when the rotation does not generate significant centrifugal force, like in the case of disks at stationary or very low RPM (Revolution Per Minute) situations. With high rotational speed, which generates significant centrifugal force, the centrifugal force should be taken into considerations as well. Usually, if the centrifugal force becomes the dominate force in this process, a conformal film profile will be generated; on the other hand, dominance of capillary and gravitational forces results in a planner profile.[239] Even though, the force of gravity is usually discounted due to the fact that this force becomes insignificant for gap widths of 5000 μm or less.[239] 5000 μm

is an extremely large dimension in fabrication technology; gaps usually have width of just a few microns or less.

A.2.3.1.2. Spin Rate Considerations

The concept of critical width has been suggested by L. E. Stillwagon to account for interaction of these two main forces: centrifugal and capillary.[239] The critical width, w_c, is defined as the width for which the centrifugal force is equal to capillary force. It has been observed that for gap widths larger than w_c the film profile, resulting from a spin coating process, is conformal. On the other hand, for gap widths much less than w_c the film profile is more planner. This is another indication that spin coating performs much better for local planarization than for global planarization. A formula has also been suggested for determining the critical gap, w_c, as a function of angular velocity ($\frac{\text{radian}}{\text{Sec.}}$) and the distance form center of rotation:[239]

$$w_c = \left(\frac{16\,\gamma\,h}{\delta\,\omega^2\,r}\right)^{\frac{1}{3}} \quad \boxed{\text{Eq. A.1.22}}$$

Where,

γ = Internal tension.

h = Depth of the gap.

δ = Density of the material used for coating.

ω = Angular velocity.

r = Radial position from center of rotation.

If typical values for the variables in the above equation are chosen, then the value of 50 μm will result for w_c. That is, if γ is set to 30 dyn/cm, ω to 420 rad/sec, r to 2.5 cm, and h is chosen to be equal to 1μm, then the calculation results in 50 μm for w_c.[239] Here, it should be reminded that this result is for Newtonian fluids; nevertheless, the result are applicable to non-

Newtonian fluids with good consistency.[239] Also, it should be noted that the above discussion is for isolated gaps and not for closely spaced gaps. In case where the space between the gaps is smaller than the gap itself, no clear consensus exist on what distance should be taken as the gap size; ie. the distance between the gaps, the gaps width itself, or any combination of the two.

A.2.3.1.3. Organic Materials in Spin Coating

Organic materials are good candidates for spin coatings. This is partially due to their high viscosities. Among the most popular organic materials used for spin coating are:

- Polyamid[227]
- Triarylsulfonium hexafluoroantimonate[239]
- 3,4 epoxycyclohexylmethyl-3,4-epoxyclohexane (epoxy A)[239]

The major disadvantage of using the organic materials in semiconductor industry is their low thermal stability. Most organic materials available today melt or decompose below 500°C.[227] Table A.10 compares the properties of Hitachi's PIQ polyamid with some of the other non organic materials used for coating.[227]

A.2.3.2. BOROPHOSPHOSILICATE Glass (BPSG) Planarization

Another popular technique for planarization is deposition of borophosphosilicate glass (BPSG). A new technique proposed by Warner Kern and Jim Hartman presents the possibility of simultaneous deposition and fusion flow planarization of BPSG in a specially designed CVD reactor.[228] This method operates at temperatures in the range of 800-875°C for a very short period of time (less than 15 minutes) to both deposit the glass, and complete the process of fusion flow planarization. Therefore, this process causes very little damage to the lower

layers. The only disadvantage of this method is its requirement for 800-875°C operating temperatures. Even though, these temperatures are needed for very short period of time; accumulated effects of planarization for several layers could add up to destroy the devices built in the lower layers.

A new planarization process has recently been proposed for SiO_2 films.[240] This process combines the PECVD and Reactive Ion Beams (RIB) procedures in order to deposit planarized SiO_2 films. The reactor for this process is shown in Fig. A.11.[240]

Table A.10. "Comparison Between Properties of PIQ and Some Inorganic Materials"[227]

Material	Coefficient of thermal expansion $X10^6$ (°C)	Young's module of elasticity $X\ 10^4$ ($gf\ cm^{-2}$)	Tensile Strength $X\ 10^4$ ($gf\ cm^{-2}$)	Thermal Conductivity $\frac{mcal}{cm\ s\ °C}$	Melting Point (°C)	Dielectric constant	Dielectric breakdown strength ($V\ cm^{-1}$)	Volume resistivity (Ω cm)
PIQ	20-70	300	1.7[a]	0.4	450--500[b]	3.5-3.8	10^6	10^{16}
Si	2.3	1.6	120	72-340	1420	11.7-12	10^5	-
SiO_2	0.3-0.5	0.7	1.4	5	1710	3.5-4.0	10^6-10^7	$>10^{16}$
Si_3N_4	2.5-3	1.6	6.4	28	1900	7-10	10^6-10^7	10^{12}
Al_2O_3	9	3.7	28	78	2050	7-9	10^5	10^{14}
Al	25	70	0.7-1.4	570	660	-	-	$2.5X10^{-6}$

[a] Limit of tensile strength.

[b] Temperature of decomposition.

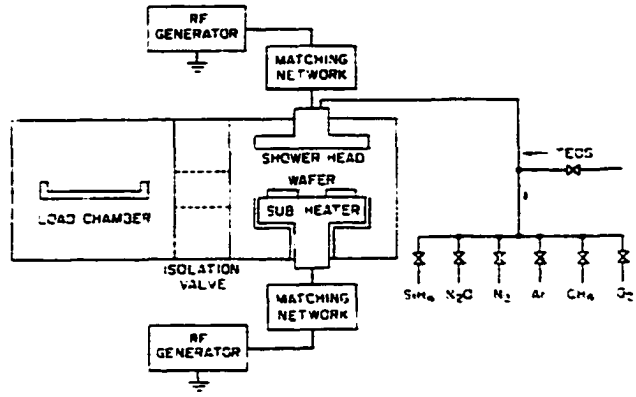


Fig. A.11. A CVD reactor proposed by Huo et al. for Planarization of SiO_2 films.[240]

In the above CVD reactor (designed for this process) the RF power supplier, connected to both the substrate and the shower head, has a frequency of 13.56 MHz and the maximum output power rating of 600 to 700 W.[240] As it can be seen in Fig. A.11, there are six gases (SiH_4, N_2O, N_2, Ar, CH_4, O_2) in addition to tetraethylorthosilicate (TEOS) that are utilized in this reactor. Most of the reactor's physical variables, such as pressure, RF power, flow speed, and the deposition timing are controlled by the reactor's own microprocessor, in order to precisely control all these variables. In this process, typically the substrate temperature is kept at around 320-370 ^oC.[240] Unlike the conventional methods, where the shower head has a negative bias and the substrate is grounded, in this process a negative bias is applied to the substrate. By biasing the substrate, one increases the potential difference between the substrate and the plasma. It has been reported that this potential difference could be as much as 25 times greater than the potential difference of an unbiased substrate.[240] The larger the potential difference between the substrate surface and the plasma, the larger the energy of ions that are bombing the substrate surface. This greater energy leads to better step coverage.[240] It has been shown that the best compromise between the least amount of radiation damage to devices

already built on the substrate and the degree of substrate planarization could be achieved at around -480.0 V of substrate bias, for the reactor shown in Fig. A.12.[240] The biggest disadvantage of this method over other methods is the radiation damage. Fig. A.11 presents a sample of a planarized substrate with this method.[240]

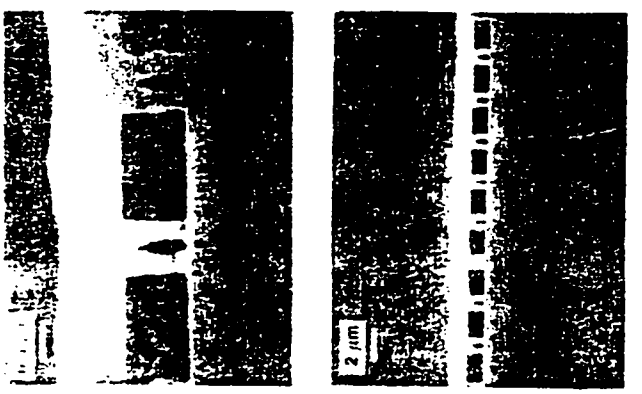


Fig. A.12. "SEM micrographs showing cross sections of planarized SiO_2 films by employing SiH_4 and N_2O precursors"[240].

A.2.3.3. Planarization using Amorphous Carbon (a-C:H)

Another PECVD procedure utilized for planarization purposes is the PECVD of amorphous carbon (a-C:H) films.[221,241-243] Due to the low bias potential (usually less than 25 V) used in this procedure for the deposition of amorphous carbon (a-C:H) films, little radiation damage to the lower lower is caused. Moreover, in this method the film of amorphous carbon (a-C:H) can be deposited at very low temperatures (usually around 50°C).[221] It is apparent that such low temperatures do not destroy the previously built layers; therefore, this method, which is in its infancy at the present time, has great potential for utilization in 3DI technology.

One other technological advantage of this method is it's high deposition rate, even in low temperatures. The deposition rates of 300 to 800 nm per minute have been reported for this technique. Nevertheless, it should be noted that a hardening step after deposition may be required in order to prepare the deposited materials for subsequent steps.[243]

It should also be mentioned that the deposited films with this technique are compatible with a majority of resist systems.[221] This fact presents a great technological and economical advantage for this technology, since there is no need to develop a new resist system for this method. In addition, it has been reported that this technique has been effective to produce a good local and global planarization profile.[221]

A.2.3.4. Sacrificial Etchback (SE) Planarization Technique

Sacrificial Etchback (SE) presents yet another popular method for planarization.[221, 229-230] This planarization technique is based on the fact that the resist materials are better planarize than the insulator layers themselves. Therefore, after a thick coating of insulator film is deposited; the resist material is spun on top of the deposited insulator. Later, using Reactive Ion Etch technique, the resist and the insulator itself are etched back by 1:1 ratio. Using this way of etching back all the resist, a planarize surface of the insulator is achieved at the same time.

Even though, at the first glance this method seems to be flawless; there are a few potential problems associated with this method as well.[221] The main problem associated with this method is that it can not provide global planariztion. Utilizing multiple resist layers reduces or eliminates most problems associated with this method and provide "a perfect planarization"[229] procedure.[229-230] Fig. A.13. presents schematic diagram of a planarization process using several methods including multiple resists, biased deposition, and sacrificial etchback processes.[229] This process, shown to have excellent results, is described in detail by Shinji et. el.[229]

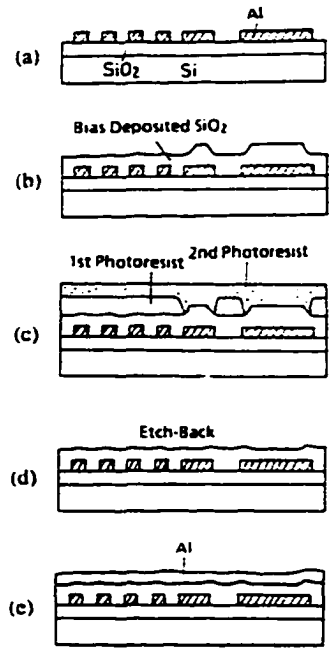


Fig. A.13. Schematic diagram of dielectric planarization process, using bias sputtered SiO_2 and etchback.[229]

A.2.3.5. Chemical-Mechanical Polishing (CMP)

Finally, the Chemical-Mechanical Polishing (CMP) is the last planarization technique to be reviewed here.[221, 231-236] This technique could be utilized to planarize oxide, metal, and polysilicon surfaces. This technology can achieve better global planarization than local planarization. The performance of this technique for different feature sizes has been studied by Uttecht et al.[236] A polishing machine is shown in Fig. A.14.[244]

Again, there are a few problems associated with this technique, too.[221, 229-236] One of the biggest problems is over-polishing. This is due to difficulty in controling an exact polishing depth. Contamination is another important problem in this technique. Finally, one should be very careful to prevent mechanical damage to the substrate that results from mis-alignment.

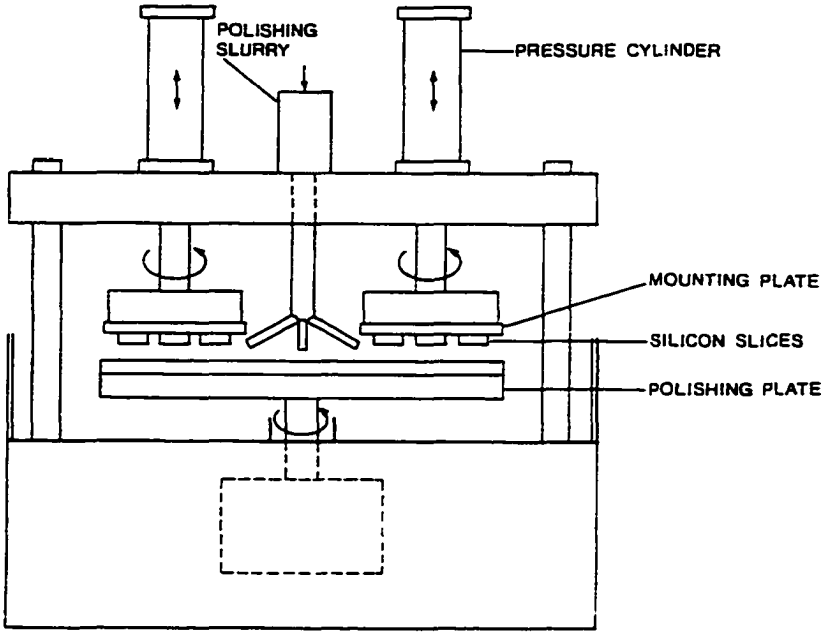


Fig. A.14. Schematics of a polishing machine.[244]

A.2.4. Recrystallization Techniques

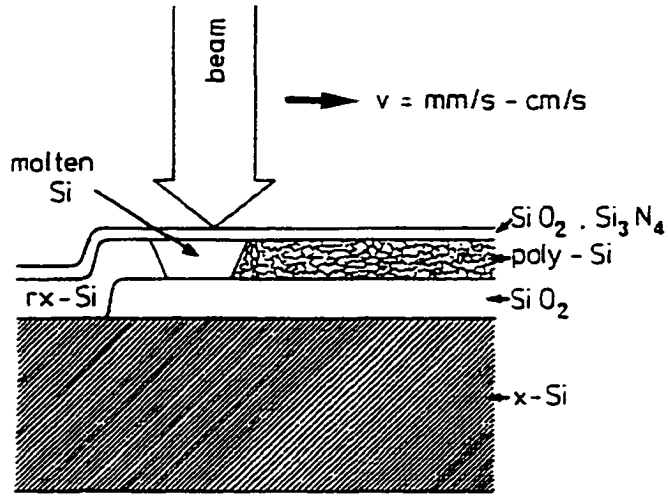
As it has been mentioned earlier, due to low temperature requirement of 3DI technology, most materials should be deposited at low temperatures. However, semiconductor materials deposited at low temperatures have amorphous or polysilicon structures. The semiconductors with amorphous or polysilicon structures have inferior electrical characteristics

in comparison with single crystalline semiconductors' electrical characteristics. To improve the electrical characteristics of these materials without damaging the previously built layers, a few new techniques have been developed in recent years.[245-249, 250-255]

The distinctive feature of these techniques is their special thermal budget. The thermal budget of these processes should be adequate to melt the poly crystalline SOI layer and impotent enough not to deteriorate the underlaying layers. Several heating processes using various heating instruments such as lasers, electron beams, lamps, and strip heaters have been shown to meet this thermal budget requirement.[251-255] The main recrystallization mechanism is the same in all these cases; a high energy beam is utilized to melt the small region (zone) of the substrate. This high energy beam is slowly moved around the substrate until the entire substrate surface has been swept. The recrystallized layer has characteristics very close to a single crystal semiconductor; therefore, the devices built on this layer should have just as good characteristics as those built on a single crystalline semiconductor.[251] Fig. A.15 Presents a visual description of the main mechanism used by all of these techniques.[251, 256-257]

A.2.4.1. Seeding Technique

The above figure also reveals another important technique utilized in these recrystallization methods. This technique, called "seeding", uses the crystal structure of lower layer as a reference for recrystallization of upper layer. That is, the top polysilicon layer is connected with the lower (single crystal) layer by etched windows in the insulator layer. When the top polysilicon layer is molten, a small part of the single crystal layer underlying the insulator layer melts as well. This ensures that upon recrystallization, the recrystallized layer will have the crystal orientation of underlying layer, due to that fact that recrystallized layer is seeded by the crystal of the underlying layer.[256-257] Fig. A.16 clearly demonstrates the concept of seeding using SEM micrograph of a seeding window cross-section before and after recrystallization.[258]



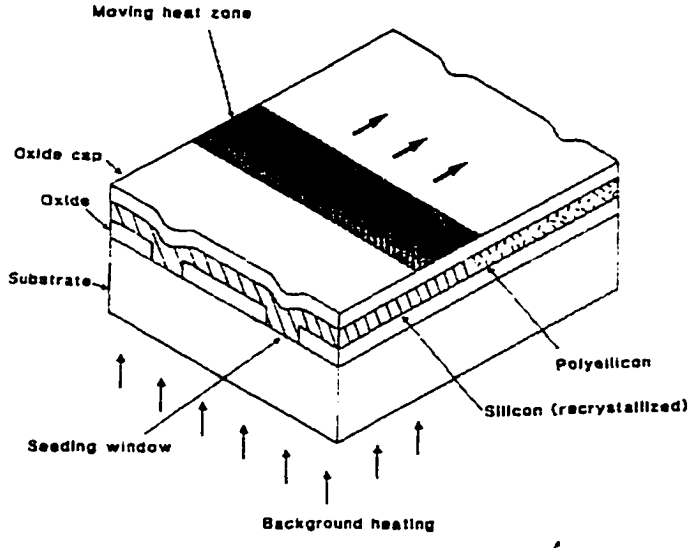


Fig. A.15. Basic mechanism of recrystallization techniques.[256-257]

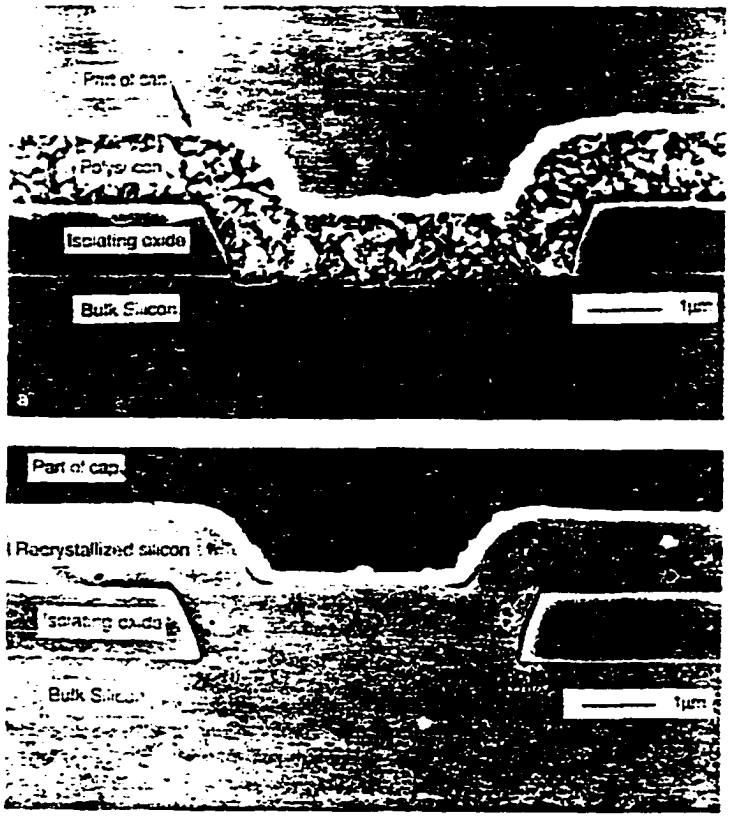


Fig. A.16 SEM cross-section of a seeding window before (top) and after (bottom) recrystallization.[258]

A.2.4.2. Control of the Recrystallization Process

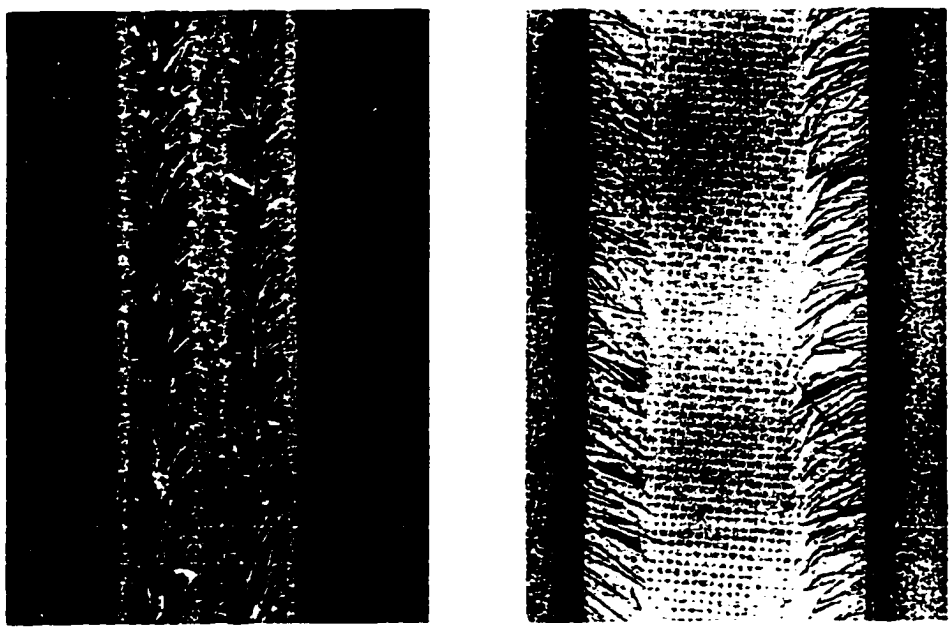
In order to produce defect free materials with this method, the recrystallization process should be controlled very carefully. The key to successful control of this process is to regulate the temperature profile in polysilicon.[250, 259-260] Three strategies have been suggested to control the temperature profile of the region under the beam.

The first strategy is to shape the intensity profile of the beam. For example, it is known that the gussian beam profile produces a molten region with a circular shape and a convex trailing edge (the liquid-solid interface is convex). Due to the fact that crystal growth always occurs normal to liquid-solid interface[261], the recrystallization process starts from the edges and proceeds towards center of the scanned area. As a result, many polysilicon grains act as the seeds for the recrystallization process. This causes a formation of several small crystals, each with different crystallographic direction. The formation of a "chevron like" pattern seen in Fig. A.17 results from this fact.[261]

To overcome this problem, several different beam profiles have been suggested.[250] Two of the most common ways used to modify the beam profile for this technique are the superimposing of a splitted beams partially[261] and passing the beam through a cylindrical lense.[250] The latter method results in an elliptically shaped beam, which is currently the most popular method used in the laser recrystallization technique. Other methods for reshaping the beam profile are presented in Fig. A.18.[250]

The second technique for controlling the beam recrystallization process is to engineer a desirable absorption characteristics on the SOI film. This is usually done by depositing different thicknesses of anti-reflection films over SOI film.[250, 261-262] The anti-reflection / absorbing capping layer is made of oxide / nitrite sandwich. By modifying the thickness of

each layer, the desired heat profile is created on top of the SOI layer. These capping layers are usually patterned in rows by lithographical methods to produce a concave trailing edge for the molten zone; therefore, causing the seeding process to start from the seeding holes. Fig. A.19 presents a wide variation of this method practically used in different institutions.[250]



a b

Fig. A.17. "Optical micrograph of dual-beam argon-laser recrystallized polysilicon layers showing the grain structure after one scan with a) insufficient power density in the middle part of the scan and b) optimal power density."[261]

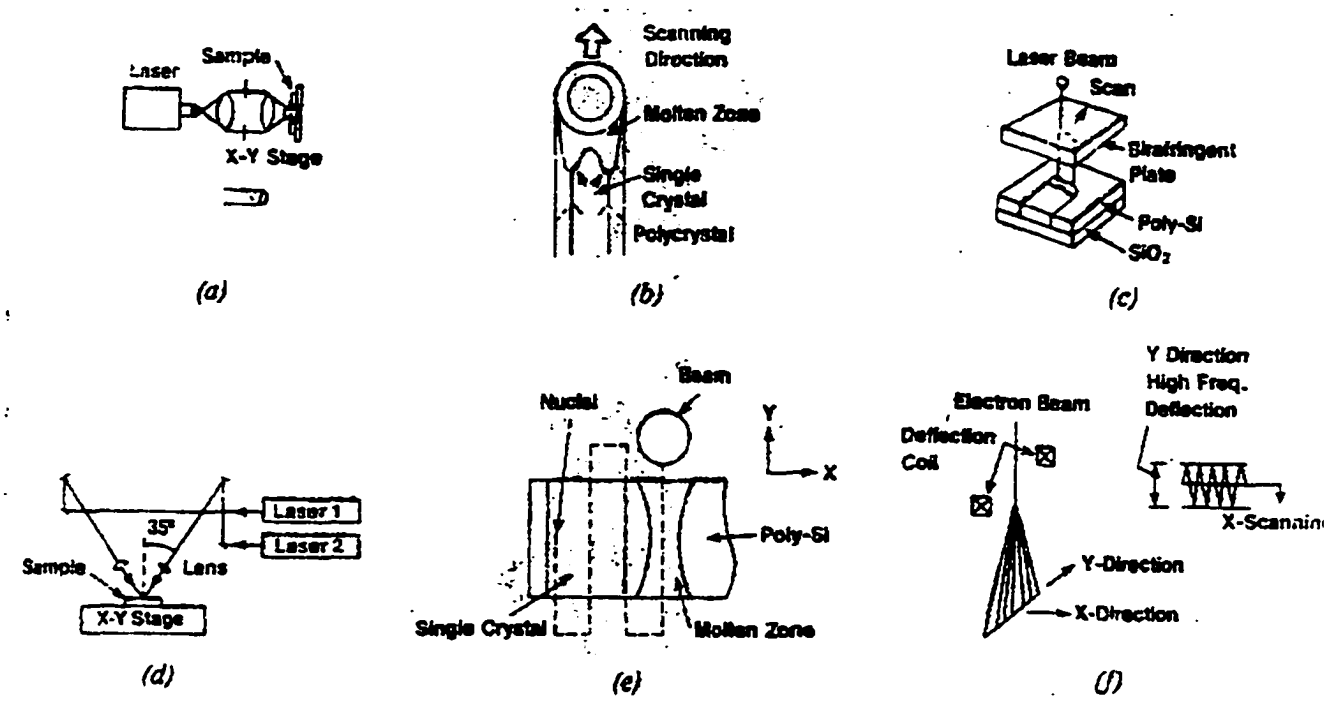


Fig. A.18. Various methods employed to modify the intensity profile of the beam spot. "(a) beam profile change achieved with a mask (Stanford Univ., single crystal, 45 μm X 50 μm ; (b) donut-type beam produced by oscillation mode modification (Fujitsu, crystal 600 μm long); (c) beam splitting (NEC, crystallized area 20 μm X 1000 μm); (d) double laser beams (Fujitsu, 20 μm, Matsushita, 1800 μm); (e) e-beam oscillation - oscillatory growth methods (AT&T Bell Labs, 50 μm X 50 μm); (f) quasilinear electron beam (Toshiba and Tokyo Inst. of Technol., 300μm)."[250]

Finally, the third method for creating a desirable thermal profile on a SOI layer is to change the heat transfer characteristics by engineering the physical structure of a SOI layer. Fig. A.20. presents various techniques that use this method for creating desirable thermal characteristics on a SOI layer. Among the methods mentioned here, the first method is the most appropriate choice for 3DI technology. There are two main reasons for this selection.

First, The changing beam profile method requires no additional processing on the SOI layer. As it has been mentioned earlier, each processing step on the SOI layer reduces the yield. Secondly, this method does not alter the topology of the SOI layer; therefore, subsequent planarization steps could better planarize the surface topology.

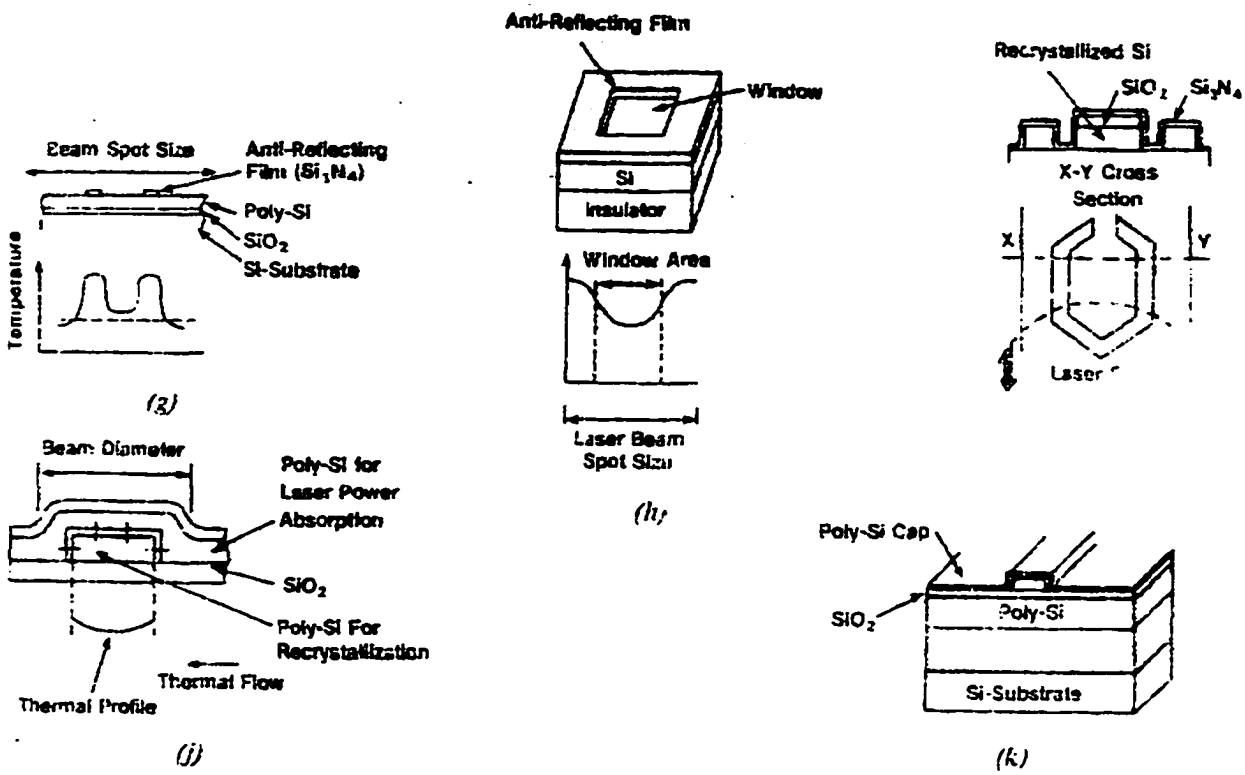


Fig. A.19. Various methods that use anti-reflection patterning to modify the heat characteristics of SOI layer. "(g) stripe-patterned, antireflecting, thin film (CNET- France, 20 μm X 400 μm, and Mitsubishi, 20 μm X 1800 μm); (h) patterned antireflecting, thin film (Fujitsu); (i) changing the reflectivity, i.e., moated island approach (General Electric, 18 μm X 50 μm); (j) indirect heating(Fujitsu, 20 μm X 60 μm); and (k) double polysilicon layer recrystallization (Sharp)."[250]

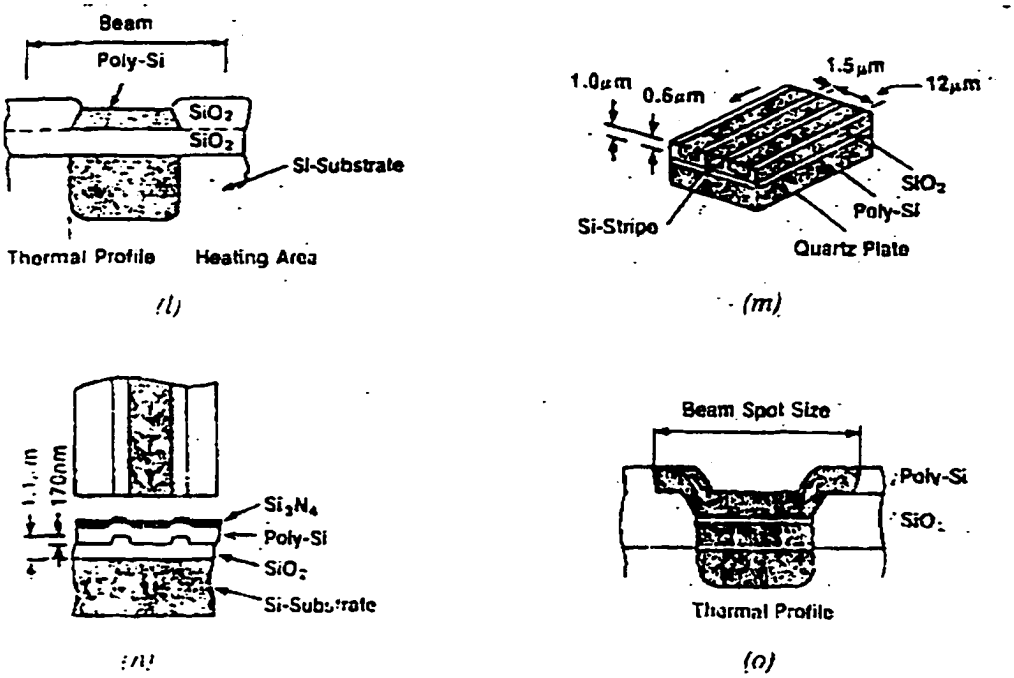


Fig. A.20. This group of methods modifies the physical structure of the SOI layer so as to achieve desirable heat transfer characteristics. "(l) LOCOS island edge heating (TI, HP, Mitsubishi, Matsushita, Sharp, 10 μm X 50μm); (m) buried stripe structure (NEC, 12 μm X 500 μm); (n)relief structure of SiO_2 to control thermal flow to the substrate (Mitsubishi 8 μm X 200 μm; and (o) heat sink Structure (Fujitsu)."[250]

To achieve the best results a combination of these methods may be used. For example, an elliptical laser beam could be further enhanced by stripes of antireflection layers, as shown in Fig. A.21. These antireflection layers are placed at a distance on both sides of the seeding holes.

A.2.4.3. Scanning Techniques

Different methods of scanning and seeding have been developed in the recent years.[261, 263-264] In one of the most interesting procedures, an elliptical laser beam scans over periodically arranged seeding holes. These seeding holes form parallel lines, as shown in Fig. A.22. The seeding holes in this figure is discontinuous; however, continuous strips format could be used for seeding window as well.

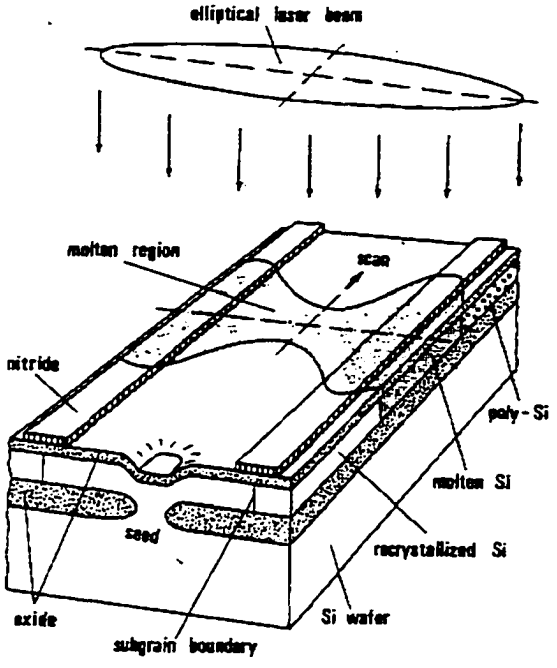


Fig. A.21. A combination of the beam shaping method and modification to heat transfer characteristics using antireflection techniques are utilized to get the optimum results.[261]

As it can be observed from Fig. A.22, the elliptical spot is scanned parallel to stripes while the axis of the ellipse makes a 45° angle with this direction. This is done to encourage crystal growth in a [110] direction that has the best correspondence to (111) plane.[261] It has been reported that recrystallization close to [111] direction produces "the most stable lateral epitaxial growth".[261, 265] A recrystallized sample prepared with this recrystallization method is shown in Fig. A.23.

In order to reveal the crystallographic orientation of the sample in Fig. A.23, the capping layer is first patterned with circular holes and is then etched with an anisotropic wet etch. Moreover, a Secco-etch is performed on the sample at the end. The grain boundaries can be detected by regular shape of squares, which indicate a perfect (100) silicon surface.[261]

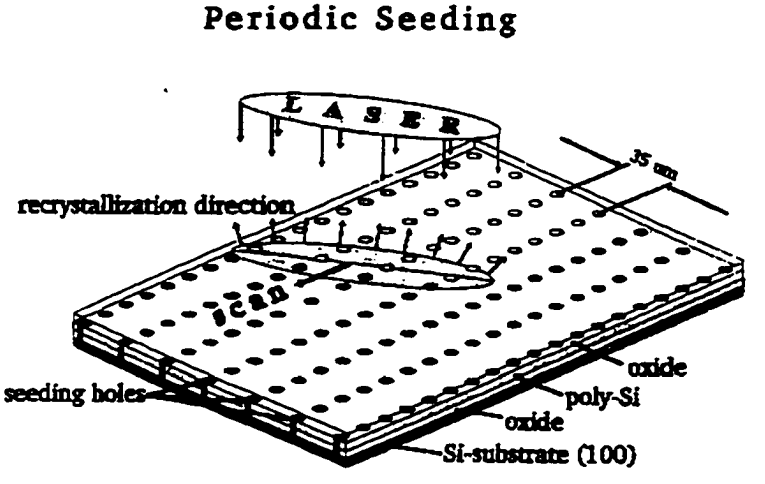


Fig. A.22. "Schematics of laser recrystallization using a parallel arrangement of discontinues seeding windows."[261]

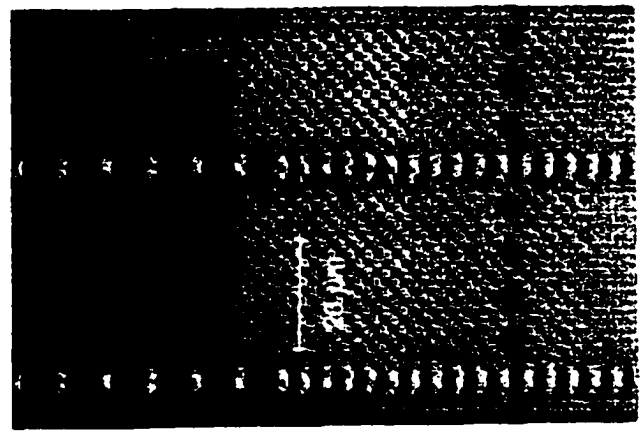


Fig. A.23. Optical micrograph of a SOI layer that is recrystallized by the method shown in Fig. A.21. The crystallographic orientation can be detected by the etch squares between the seeds.[261]

A schematic diagram of a system designed based on this technique for high through put is shown in Fig. A.24. As it can be seen, a relatively high power continuous wave argon laser (20-30W) is utilized as the source. The laser beam generated by this source is passed through a cylindrical lense to generate an elliptical shaped laser beam. Also it should be noted that in this system the substrate is kept at around 500 - 600°C.[261] Since it only takes 4 minutes to completely recrystallize a layer on a 4" substrate, the effect of temperature on underneath layers is negligible.

A.2.4.4. A Note About Different Beam Sources

As mentioned before, many beam sources can be used for recrystallization purposes.[251-255] Moreover, the source of the beam plays very important role in the

recrystallization mechanism and in the recrystallized material.[261] For example, the electron beams could be easily deflected by electric and magnetic fields; whereas, light sources can not be reflected by electric or magnetic fields directly. Therefore, these unique characteristics should be considered for choosing the recrystallization technique.

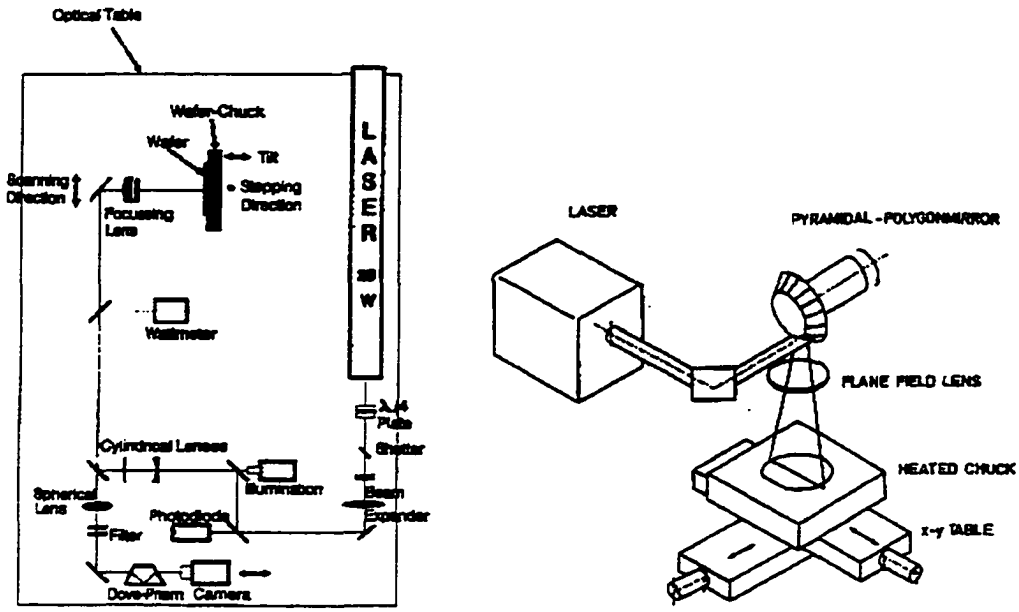


Fig. A.24. Schematics of laser recrystallization machines.[261]

There are differences between different laser sources, as well. For example, the radiation of an Argon laser still gets completely absorbed even in a reasonably thin polycrystalline silicon; whereas, the radiation of a CO_2 laser (with 10.6 μm wave length) is only absorbed by the silicon's free electrons.[261] This is due to the differences in the wave length of the two lasers and the energy bandgap of the silicon itself. Taking this in consideration, one sees that most of the energy of the Argon laser is absorbed in top layer (which is being recrystallized) while most of the energy of the CO_2 laser will be absorbed by

layers underneath the top layer. This degree of absorption by lower layers could generate enough heat to destroy the lower layers by redistributing their impurities. Therefore, in cases where CO_2 laser beam sources have to be utilized, thick capping layers are placed on top of the silicon and the SOI layers should have larger oxide thicknesses. This tactic ensures that most of the power will get absorbed in the top layer.[266]

Other beam sources have advantages and disadvantages of their own. For example, e-beam recrystallization may cause severe radiation damage to underlaying layers; even though, it can be moved across the substrate easily by electric and magnetic field the same way the beam is moved around in a CRT tube[245, 267-268]. Non-coherent and unpolarized light sources (the light generated by regular lamp) are easier to generate at high powers. However, they are not as accurate as laser beams.[269]

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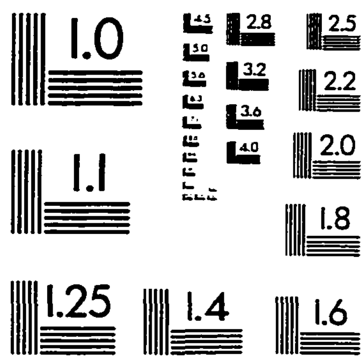
IMAGE EVALUATION TEST TARGET (QA-3)



150mm

6"

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